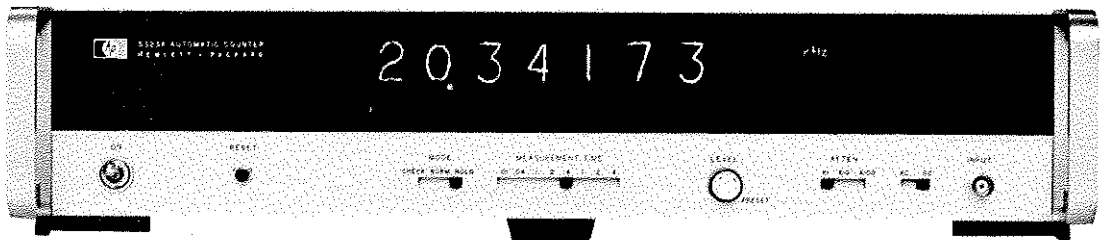


# AUTOMATIC COUNTER

## 5323A



HEWLETT  PACKARD

## **CERTIFICATION**

*The Hewlett-Packard Company certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory. The Hewlett-Packard Company further certifies that its calibration measurements are traceable to the U.S. National Bureau of Standards to the extent allowed by the Bureau's calibration facility.*

## **WARRANTY AND ASSISTANCE**

All Hewlett-Packard products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products which prove to be defective during the warranty period provided they are returned to Hewlett-Packard. No other warranty is expressed or implied. We are not liable for consequential damages.

Service contracts or customer assistance agreements are available for Hewlett-Packard products that require maintenance and repair on-site.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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## AUTOMATIC COUNTER 5323A

### SERIAL PREFIX: 936-

This manual applies directly to Hewlett-Packard Model 5323A Automatic Counters having serial prefix 936.

### SERIAL PREFIXES NOT LISTED

For newer instruments with serial prefix above 936, a "Manual Changes" sheet is included with this manual. For older instruments with serial prefix below 936, changes required to backdate the manual can be found in Section VII.

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**02841-1**                      Printed: NOV 1969

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**MANUAL CONTENT**

This manual provides operating and service information for Hewlett-Packard 5323A Automatic Counter. Information is arranged in eight sections as follows:

Section I, GENERAL INFORMATION, contains an overall instrument description, specifications, equipment supplied, available accessories, options, and instrument applications.

Section II, INSTALLATION, covers unpacking, inspection, rack installation, power and cooling requirements, connections for remote programming, and printer operation.

Section III, OPERATION, explains how to operate the 5323A, including display interpretation for all modes of operation.

Section IV, THEORY OF OPERATION, describes the overall theory of operation. Integrated circuit operation and special circuit operation are included in this section.

Section V, MAINTENANCE, provides maintenance procedures, assembly designations, recommended test equipment, in-cabinet performance checks (incoming inspection), adjustments (calibration procedures), overall troubleshooting (locating defective assembly), and removal and replacement instructions.

Section VI, REPLACEMENT PARTS, lists replacement parts by reference designator, including options, lists total quantity of each part used, and manufacturer's code and part number.

Section VII, OPTIONS, SPECIALS, AND MANUAL CHANGES, covers options available, information for special instruments where applicable, and provides information to make this manual applicable for older instruments.

Section VIII, CIRCUIT DIAGRAMS AND SERVICE INFORMATION, contains schematic diagrams and component locators for all assemblies, operation of each assembly including waveforms and voltages. Adjustment and troubleshooting information are included in this section.

**ADDITIONAL MANUALS**

To order additional operating and service manuals, contact your nearest Hewlett-Packard Sales and Service Office. Give complete model name, and 8-digit serial number. The serial number plate is on the rear panel (see Section I for serial number system). This manual's HP part number is the last item listed in Table 6-1. Comments on this manual are welcome at any Sales and Service Office.

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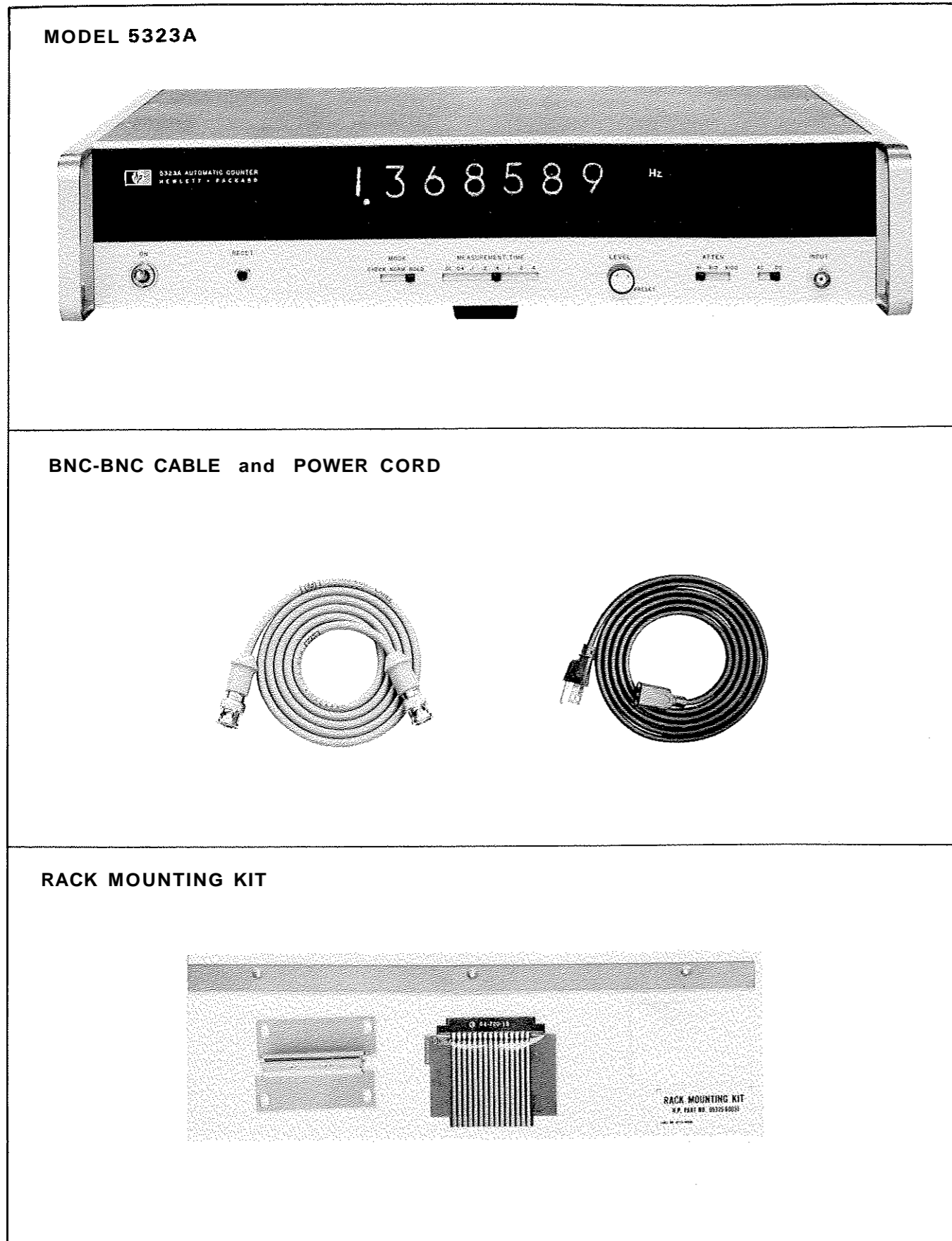
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Figure 1-1. Model 5323A and Accessories



**SECTION I**  
**GENERAL INFORMATION**

**1-1. DESCRIPTION**

1-2. The 5323A Automatic Counter measures frequency with automatic range selection and constant resolution at all frequencies from 0.125 Hz to 20 MHz.

1-3. Frequency is measured by counting an arbitrary number of input periods (X) and accurately measuring the number of clock periods (Y) during the same interval. Input frequency is then computed by dividing X by Y and multiplying the result by the clock frequency. Frequency is displayed with seven digit resolution, automatically positioned decimal point, and correct measurement units.

1-4. Display features included are: 10 percent range-switching hysteresis, and automatic blanking of non-significant digits.

1-5. Selected measurement times of: .01, .04, .1, .2, .4, 1, 2, and 4 seconds, are front-panel selectable or controlled through the REMOTE PROGRAM connector. Measurement times can be controlled by using an external gate signal, to obtain times other than those described above, any value from 0 to 4 seconds.

1-6. The Counter will measure RPM by converting input pulses per second through a X60 multiplier to events-per-minute.

**1-7. IDENTIFICATION**

1-8. Hewlett-Packard uses a two-section, eight digit serial number (on instrument rear panel) to identify instruments (000-00000). The first three digits are a serial prefix number, and the last five digits refer to a specific instrument. If the serial prefix on your instrument does not appear on the title page of this manual, there may be differences between the manual and your instrument. If there are differences, they will be described in a change sheet included with the manual.

1-9. All instruments with the same prefix are the same. The group of instruments to which this manual applies directly is identified on the title page. For older instruments (lower serial numbers), make manual changes listed in Section VII. For newer instruments, having serial numbers higher than those listed on the title page, manual change sheets are included, describing the required changes. The manual for an instrument having special electrical modifications will include an insert sheet describing those modifications. If a change sheet or special information sheet is missing, the information sheet can be supplied by any Hewlett-Packard Sales and Service Office listed at the back of this manual.

**1-10. SPECIFICATIONS**

1-11. A complete list of specifications is found in Table 1-1.

Table 1-1. Specifications

<b>RANGE:</b> dc coupled: 0.125 Hz to 20 MHz. ac coupled: 10 Hz to 20 MHz.	<b>HYSTERESIS Cont'd:</b> below 09... . This 10% hysteresis prevents unnecessary range changes due to input frequency jitter. Hysteresis may be inhibited by a rear panel switch.								
<b>MEASUREMENT TIME:</b> Selectable; 0.01, 0.04, 0.1, 0.2, 0.4, 1.0, 2.0, 4.0 s, or any time up to 4 s determined by tmc duration of an external gate signal.	<b>SIGNAL INPUT:</b> Sensitivity (min.): 0.1 Vrms sine wave. 0.3 V p-p pulse, 25 ns minimum pulse width. Sensitivity can be decreased by 10 or 100 times using the ATTENUATOR switch.								
<b>GATE TIME:</b> Automatically selected between measurement time and twice the measurement time.	<b>Impedance:</b> 1 MΩ shunted by 35 pF.								
<b>SAMPLE RATE:</b> Sum of gate time and computing time of approximately 1 ms.	<b>Maximum Input:</b>								
<b>ACCURACY:</b> ±1 count ± time base error ± noise	<table border="1"> <thead> <tr> <th>Volts</th> <th>ATTENUATOR Setting</th> </tr> </thead> <tbody> <tr> <td>120 Vrms (&lt; 1 kHz)</td> <td>X1</td> </tr> <tr> <td>250 Vrms</td> <td>X10</td> </tr> <tr> <td>500 Vrms</td> <td>X100</td> </tr> </tbody> </table>	Volts	ATTENUATOR Setting	120 Vrms (< 1 kHz)	X1	250 Vrms	X10	500 Vrms	X100
Volts	ATTENUATOR Setting								
120 Vrms (< 1 kHz)	X1								
250 Vrms	X10								
500 Vrms	X100								
<b>RANGE SELECTION:</b> Automatic.	<b>Overload Level:</b> 1.5 Vrms X ATTENUATOR settings								
<b>HYSTERESIS:</b> Range switching will automatically position the most significant digit in the first display position, except when the frequency is decreasing from 10... to 09... . In this case range switching is delayed until the input drops									

Table 1-1. Specifications (Cont'd)

<p><b>SIGNAL INPUT</b> Cont'd: Trigger Level: PRESET to center triggering about 0V, or adjustable:</p> <table border="1"> <thead> <tr> <th>Range</th> <th>ATTENUATOR Setting</th> </tr> </thead> <tbody> <tr> <td>±1V</td> <td>X1</td> </tr> <tr> <td>±10V</td> <td>X10</td> </tr> <tr> <td>±100V</td> <td>X100</td> </tr> </tbody> </table> <p>Trigger Threshold Band: &lt; 1.0 mV, referred to input at 20 MHz.</p> <p style="text-align: center;"><b>Time Base</b></p> <p><b>CRYSTAL FREQUENCY:</b> 10 MHz</p> <p><b>CRYSTAL OVEN:</b> Self-regulating solid-state type.</p> <p><b>STABILITY:</b> Aging Rate: Less than 3 parts in 10<sup>7</sup>/mo. Temperature: ≤ ±7 parts in 10<sup>8</sup>/°C. Line Voltage: ≤ ±1 part in 10<sup>7</sup> for ±10% line voltage variation.</p> <p><b>OSCILLATOR OUTPUT:</b> 10 MHz, 1.0 V p-p, 50Ω (approx.) source impedance at rear panel BNC.</p> <p><b>EXTERNAL INPUT:</b> 1.0 Vrms at a frequency of 1, 2.5, 5, or 10 MHz.</p> <p style="text-align: center;"><b>General</b></p> <p><b>DISPLAY:</b> 7-digit in-line Nixie® digital readout plus positioned decimal point, units annunciator, and RPM annunciator.</p> <p><b>BLANKING:</b> All non-significant digits will be automatically blanked if the measurement time selected on the front panel is too short to guarantee full accuracy. Rear panel switch allows all digits to be displayed without blanking if desired.</p> <p><b>DISPLAY STORAGE:</b> Holds reading and digital output constant between samples.</p> <p><b>RPM DISPLAY:</b> Rear panel switch connects an internal X60 multiplier that converts measurement from pulses per second to revolutions per minute.</p> <p><b>"ARMED" LAMP.</b> Is illuminated between time of reset and when input signal first reaches trigger level thereafter.</p>	Range	ATTENUATOR Setting	±1V	X1	±10V	X10	±100V	X100	<p><b>GATE OUTPUT:</b> 0V while gate open, +4V while gate closed. Available at rear panel BNC.</p> <p><b>RESET:</b> Front panel pushbutton switch resets the counter and causes display to be 0 Hz.</p> <p><b>AUTOMATIC RESET:</b> The counter will automatically reset to zero if the input is removed during any measurement, or if the period of the input signal is longer than twice the selected measurement time.</p> <p><b>HOLD:</b> Retains displayed information indefinitely while new measurement is made. New information is displayed immediately when "hold" is removed. A single measurement may be made by resetting from the "hold" position.</p> <p><b>SELF-CHECK:</b> Measures internal 10 MHz signal.</p> <p><b>REMOTE PROGRAMMING:</b> All front panel function controls are programmable.</p> <p><b>Control Signal:</b> Single line control for each function. Operated by DTL or TTL integrated circuits or contact closure to ground. Amplifier trigger level can be set by the level of an external ±1V input (which is multiplied by the ATTENUATOR settings: X1, X10, X100).</p> <p><b>DIGITAL OUTPUT:</b> Code: All numerals, decimal point, and unit information are available as 4-line! 8-4-2-1 coded signals. Logic "0" state approximately 0.4V at 10 mA sink; logic "1" state approximately 5V open circuit, 2.5 kΩ impedance.</p> <p><b>Print Command:</b> +5V to 0V step, dc coupled; occurs at end of measuring and computing cycle.</p> <p><b>Storage:</b> Buffer storage is provided so BCD output is held constant while next measurement is being made.</p> <p><b>Hold-Off:</b> Inhibits transfer of data to buffer storage when instrument's cycle time is less than time required for external equipment to interrogate BCD outputs. Positive inhibit +5V min., +20V max.</p> <p><b>Chassis Connector:</b> Special HP manufactured connector assembly.</p> <p><b>CONNECTORS:</b> All are BNC's except for Remote Programming (Cinch or Amphenol 57-40500-375, which mates with Amphenol 57-30500, HP 1251-0086) and Digital Output.</p> <p><b>OPERATING TEMPERATURE:</b> 0° to 50°C</p> <p><b>POWER REQUIREMENTS:</b> 115 or 230 volts ±10%, 50 to 400 Hz, 45 watts maximum. Fast circuit breaker action with internal power reset switch protects supply. Also resets when main power is turned off. No cooling fan required.</p>
Range	ATTENUATOR Setting								
±1V	X1								
±10V	X10								
±100V	X100								

Table 1-1. Specifications (Cont'd)

<p><b>WEIGHT:</b> Net, 14 lb (6,4 kg). Shipping, 19 lb (8,6 kg)</p> <p><b>ACCESSORIES FURNISHED:</b> Power cord, 7-1/2 ft. HP 10503A, 50Ω BNC to BNC cable, 4 ft (122 cm). Rack mount kit with P.C. extender board.</p> <p><b>DIMENSIONS:</b> 3-15/16 in. high, 16-3/4 in. wide, 11-1/4 in. deep (88,2 x 425 x 286 mm).</p>	<p>NOTE: DIMENSIONS IN INCHES AND (MILLIMETERS) (A) EIA RACK HEIGHT INCLUDING FILLER STRIP (B) CABINET HEIGHT INCLUDING FEET AND (C) TO EIA RACK HEIGHT (D) REAR APRON HEIGHT</p>
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**1-12. INSTALLATION AND OPERATION**

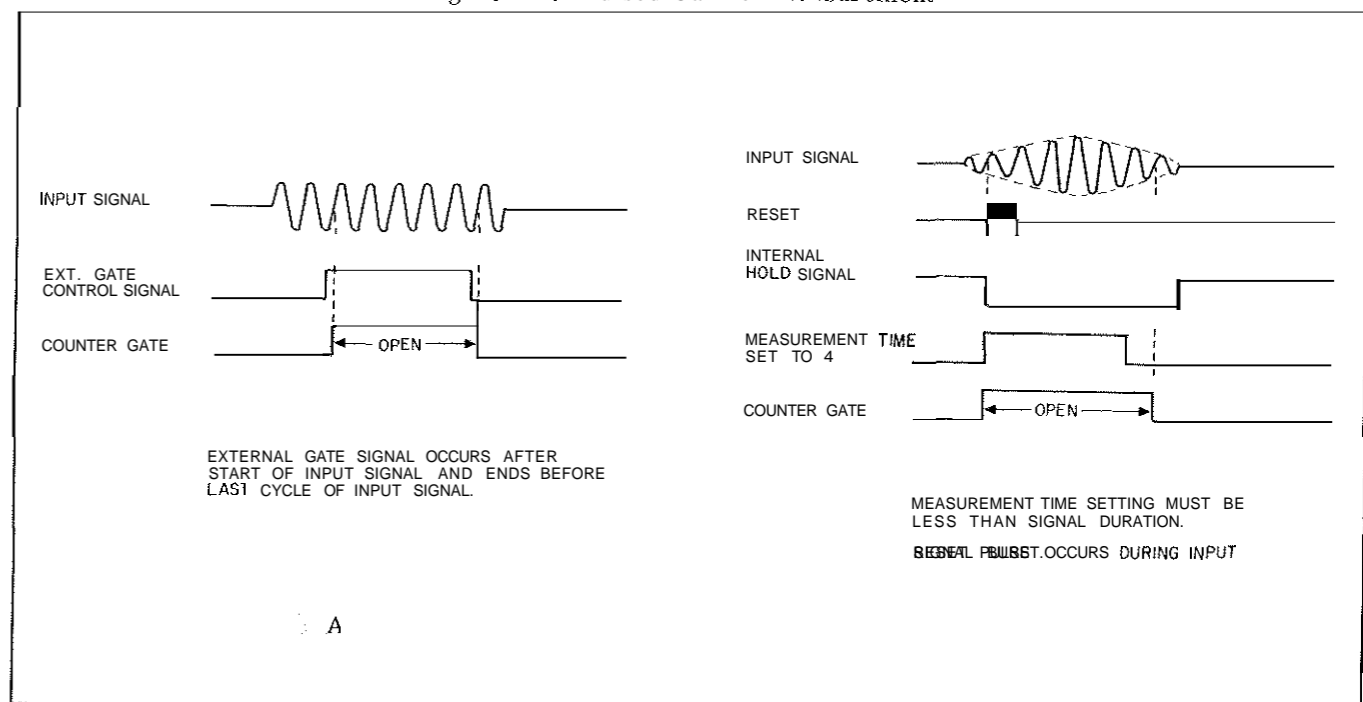
1-13. Installation and operation procedures are described in Sections II and III of this manual. Remote programming and use of the HP 5050B Digital Recorder are included in Section II.

**1-14. APPLICATIONS**

1-15. The Automatic Counter measures frequency directly from 0.125 Hz to 20 MHz. For tachometry applications, an internal X60 multiplier converts data from pulses per second to events per minute.

1-16. The Counter can be used to measure the carrier frequency of a pulsed signal (tone burst) without the use of a transfer oscillator by one of two methods. First is to apply an external gate signal and, as long as the gate signal is removed before the burst ends, the counter will measure the carrier frequency. Second is to set MEASUREMENT TIME switch to a time known to be shorter than the burst and the MODE switch to HOLD. Then apply a reset pulse to the Counter sometime between bursts. The 5323A will start counting when a burst starts, and will stop before the burst ends. The two modes of operation are shown in Figures 1-2A and 1-2B.

Figure 1-2. Pulsed Carrier Measurement



1-17. **EQUIPMENT SUPPLIED  
AND AVAILABLE**

Table 1-2. Equipment Supplied

DESCRIPTION	HP PART NO.
Cable: 4 ft. (122 cm) 50 ohm, male BNC connectors	10503A
Rack Mount Kit	05325-60031
Printed Circuit Extender Board	05245-6022
Detachable Power Cord: 7-1/2 ft. (231 cm) NEMA Plug	8120-0078
Fuse: Slo-Blow, 0.4A, 125V (For 230 Vac operation)	2110-0019

1-18. Equipment supplied is listed in Table 1-2. Table 1-3 lists some of the equipment available for use with the 5323A Counter.

Table 1-3. Equipment Available

DESCRIPTION	HP PART NO.
Recorder Interconnecting Cable	10524A
Digital Recorder	5050B

**SECTION II  
INSTALLATION**

**2-1. INTRODUCTION**

2-2. This section contains information on unpacking, inspection, repacking, storage, installation, remote programming, and use with the HP 5050B Digital Recorder.

**2-3. UNPACKING AND INSPECTION**

2-4. If the shipping carton is damaged, ask that the carrier's agent be present when instrument is unpacked. Inspect the instrument for damage (scratches, dents, broken knobs, etc.). If instrument is damaged or fails to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately (Sales and Service Offices are listed at the back of this manual). Retain the shipping carton and the padding material for the carrier's inspection. The Sales and Service Office will arrange for repair or replacement of your instrument without waiting for the claim against the carrier to be settled.

**2-5. STORAGE AND SHIPMENT**

2-6. **PACKAGING.** To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Your Hewlett-Packard Sales and Service Office can provide packing material such as that used for original factory packaging. Contract packaging companies in many cities can provide dependable custom packaging on short notice. Here are two recommended packaging methods:

a. **Rubberized Hair.** Cover painted surfaces of instrument with protective wrapping paper. Pack instrument securely in strong corrugated container (350 lb/sq. in. bursting test) with 2-inch rubberized hair pads placed along all surfaces of the instrument. Insert fillers between pads and container to insure a snug fit.

b. **Excelsior.** Cover painted surfaces of instrument with protective wrapping paper. Pack instrument in strong corrugated container (350 lb/sq. in. bursting test) with a layer of excelsior about six inches thick packed firmly against all surfaces of the instrument.

2-7. **ENVIRONMENT.** Temperature limitations during storage and shipment should be limited as follows:

- a. Maximum temperature: +75°C (167°F).
- b. Minimum temperature: -40°C (-40°F)

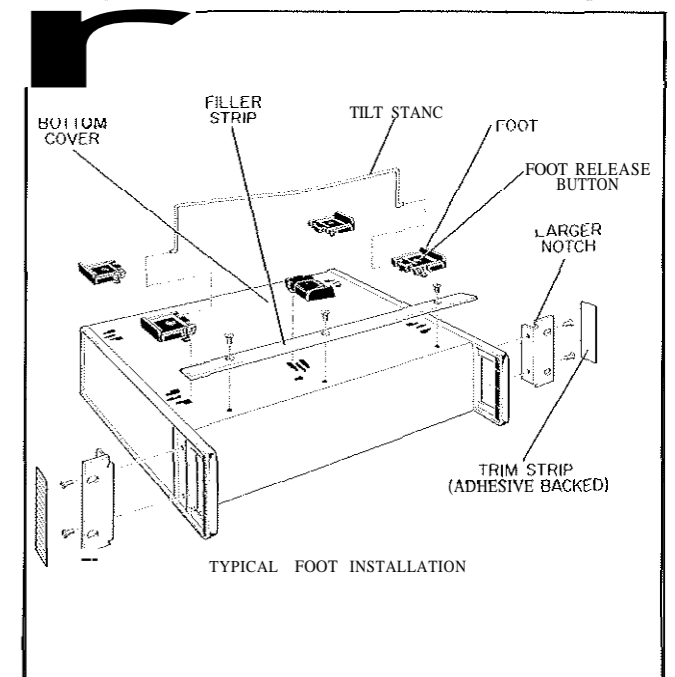
**2-8. RACK INSTALLATION**

2-9. The instrument is ready for bench operation as shipped from the factory. Additional parts necessary

for rack mounting are packaged with the instrument. To convert for rack installation, refer to Figure 2-1 and proceed as follows:

- a. Remove feet (press the foot-release button, slide foot toward center of instrument, and lift off).
- b. Remove adhesive-backed trim strips at front end of sides.
- c. Attach filler strip along bottom edge of front panel.
- d. Attach flanges to front end of sides (larger corner notch toward bottom of instrument). Instrument is now ready to mount in standard rack.

Figure 2-1. Conversion for Rack Mounting



**2-10. POWER CONNECTION**

2-11. **LINE VOLTAGE.** The Counter may be operated from either 115 or 230 volt ( $\pm 10\%$ ) power lines. A slide switch on the rear panel permits quick conversion for operation from either voltage. The Counter is supplied with a 115 volt fuse; be sure to replace the fuse for 230 volt operation; see Table 2-1.

**CAUTION**

Before plugging the instrument into the AC power line, be sure the slide switch is properly positioned.



Table 2-1. 115/230 Volt Conversion

CONVERSION	115 VOLT	230 VOLT
Slide Switch	Left (115)	Right (230)
AC Line Fuse	0.8 Ampere Slow-Blow (HP 2110-0020)	0.4 Ampere Slow-Blow (HP 2110-0019)

2-12. POWER CABLE. The Counter is supplied with a detachable three-wire power cable. To install:

a. Connect flat plug (three conductor female connector) to rear panel AC line connection.

b. Determine AC line voltage in use. Use a narrow blade screwdriver and set rear panel 115/230V switch to same as line voltage in use.

c. Connect plug (two-blade with round grounding pin) to three-wire (grounded) power outlet. Exposed portions of instrument arc grounded through plug. When only a two-blade outlet is available, use HP adapter 1251-0048 and connect short wire from side of adapter to ground.

**2-13. COOLING**

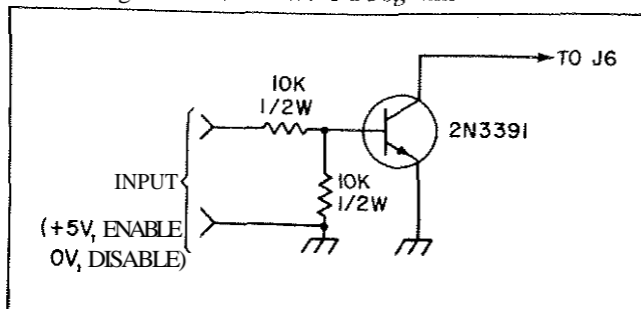
2-14. The Automatic Counter does not require a cooling fan. Adequate ventilation should be provided to maintain the temperature below +50°C.

**2-15. REMOTE PROGRAMMING**

2-16. All controls except the input attenuator, trigger level, and AC/DC coupling selector can be remotely programmed by contact closure to ground, by saturated NPN transistor, or by DTL or TTL integrated circuits.

To ensure proper operation in automatic systems, remote controls override the manual switches. Remotely programmable operations are: reset, self-check, measurement time step, measurement time interval from 0 to 4 seconds (duration equal to remote external gate command), HOLD, blanking inhibit, and hysteresis inhibit. A typical NPN transistor circuit is shown in Figure 2-2.

Figure 2-2. Remote Program Circuit



2-17. LEVEL control can be remotely set by applying a dc voltage equal to the desired triggering level (divided by input attenuator setting). LEVEL input voltage is ±1 volt multiplied by the input attenuator setting (X1, X10, X100).

2-18. Table 2-2 lists the pin assignments for J6, the remote program connector, mounted on the instrument rear panel. Wire colors, interconnection data, and levels are also indicated.

**2-19. DIGITAL RECORDER**

2-20. BCD output to drive the HP 5050B Digital Recorder are provided at A11J1 (DIGITAL RECORDER, rear panel of instrument). Pin assignments and BCD weighting for the connector signals are shown in Table 2-3.

2-21. A hold-off voltage from +5 to +20V will prevent the counter from resetting and taking a new measurement. When the Digital Recorder completes its cycle, this hold off is removed and the counter makes a new measurement.

Table 2-2. Connections to Remote Program Connector, J6

FUNCTION	PIN NO.	WIRE COLOR	CONNECTS TO*	REMARKS
15V	1	Wht-Blk	A16(13, 14)	-----
LEVEL	2	Wht-Brn	A2(3, C)	±1V (X1, X10, X100)
GROUND	3	Wht-Red	Ground	-----
RESET	4	Wht-Orn	A3(10), J4, S1	Ground will enable.
CHECK	5	Wht-Yel	A3(E)	Ground will enable.
HOLD	6	Wht-Grn	A3(P), A11J4(11)	Ground will enable.
01	7	Wht-Blu	A6(P), A8(13)	Ground will enable.
04	8	Wht-Vio	A6(N), A8(11)	Ground will enable.
.1	9	Wht-Gra	A6(9), A8(10)	Ground will enable.
2	14	Wht-Elk-Grn	A6(K), A8(9)	Ground will enable.
.4	11	Wht-Blk-Red	A6(J)	Ground will enable.
1	13	Wht-Blk-Yel	A6(H)	Ground will enable.
2	10	Wht-Blk-Brn	A6(8)	Ground will enable.
4	12	Wht-Blk-Orn	A6(7)	Ground will enable
EXT PROG	15	Wht-Blk-Blu	A11(Blu)	Ground will disable A10 **
GROUND	19	Blk	Ground	-----
EXT GATE	20	Brn	J2, A3(L)	Ground will enable A3 Board.
GATE OUT	21	Orn	53, A8(R)	0V (Gate Open). 14V (Gate Closed)
PRINT	22	Yel	A8(14), A11J4 (10)	+5V (Hold-Off). 0V (Print Command)
BLANK	23	Gra	S4, A8(F)	Ground will disable
HYSTERESIS	24	Wht	S5, A11(Wht)	Ground will disable.

No Connections are Made to Pins 16 Through 18 and 25 Through 36.

\* All interconnections between J6 and components are made via the A9 Connector Board Assembly (refer to Section VIII for schematic).

\*\*The EXT PROG signal should be grounded, so that the MODE and MEASUREMENT TIME switches will be disabled. Otherwise, the switches will still control the counter operation and may not be overridden by remote programming.

Table 2-3. Digital Recorder (A11J1) Pin Functions

OUTPUT	BCD WEIGHT			
	8	4	2	1
	A11J1 PINS			
UNITS	2(U)	2(W)	2(X)	2(V)
10 <sup>1</sup>	2(S)	1(U)	1(V)	2(T)
10 <sup>2</sup>	1(P)	2(P)	2(R)	1(R)
10 <sup>3</sup>	2(M)	1(M)	1(N)	2(N)
10 <sup>4</sup>	1(J)	2(K)	2(L)	1(K)
10 <sup>5</sup>	2(J)	1(F)	1(H)	1(E)
10 <sup>6</sup>	2(D)	2(F)	2(H)	2(E)
EXPONENT	2(Y)	2(b)	2(c)	2(Z)
+5 VOLTS	1 (C, D, L, S, T, W, X, Y, Z, a, b, c) 2(C)			
GROUND	1 (A, B) 2 (A, B)			
	PRINT COMMAND		PIN 1(d)	
	PRINTER HOLD-OFF		PIN 2(a)	

1 Indicates component (top) side of A11, 2 Indicates copper (bottom) side of A11  
Mating Connector for A11J1 is (1) HP Part No. 1251-2339, (2) Cinch Jones Part No. 600-121-26.

### SECTION III OPERATION

#### 3-1. INTRODUCTION

3-2. The Counter measures frequency or RPM. The MODE switch selects NORM, CHECK, or HOLD. The MEASUREMENT TIME switch selects .01, .04, .1, .2, .4, 1, 2, or 4 seconds. The LEVEL control determines at what voltage level of the input signal together with the ATTEN switch, the input amplifier will trigger. Figures 3-2 and 3-3 describe the front and rear panel operating controls. Figures 3-4 and 3-5 provide step-by-step operating procedures for self-check and frequency measurements. Section II explains Remote Operation.

#### 3-3. INTERPRETING DISPLAY

3-4. Direct readout is provided for all measurements. The Counter automatically places the most significant digit to the left. Decimal point is positioned and measurement unit is displayed automatically. When the Hz/RPM switch is set to RPM, RPM will be displayed, otherwise MHz, kHz, or Hz will be displayed.

3-5. The BLANKING switch causes the non-significant digit(s) to be blanked when MEASUREMENT TIME selected is too short to obtain an accurate seven-digit readout. Table 3-1 lists the number of digits displayed at various time settings.

Table 3-1. Digits Display Versus Measurement

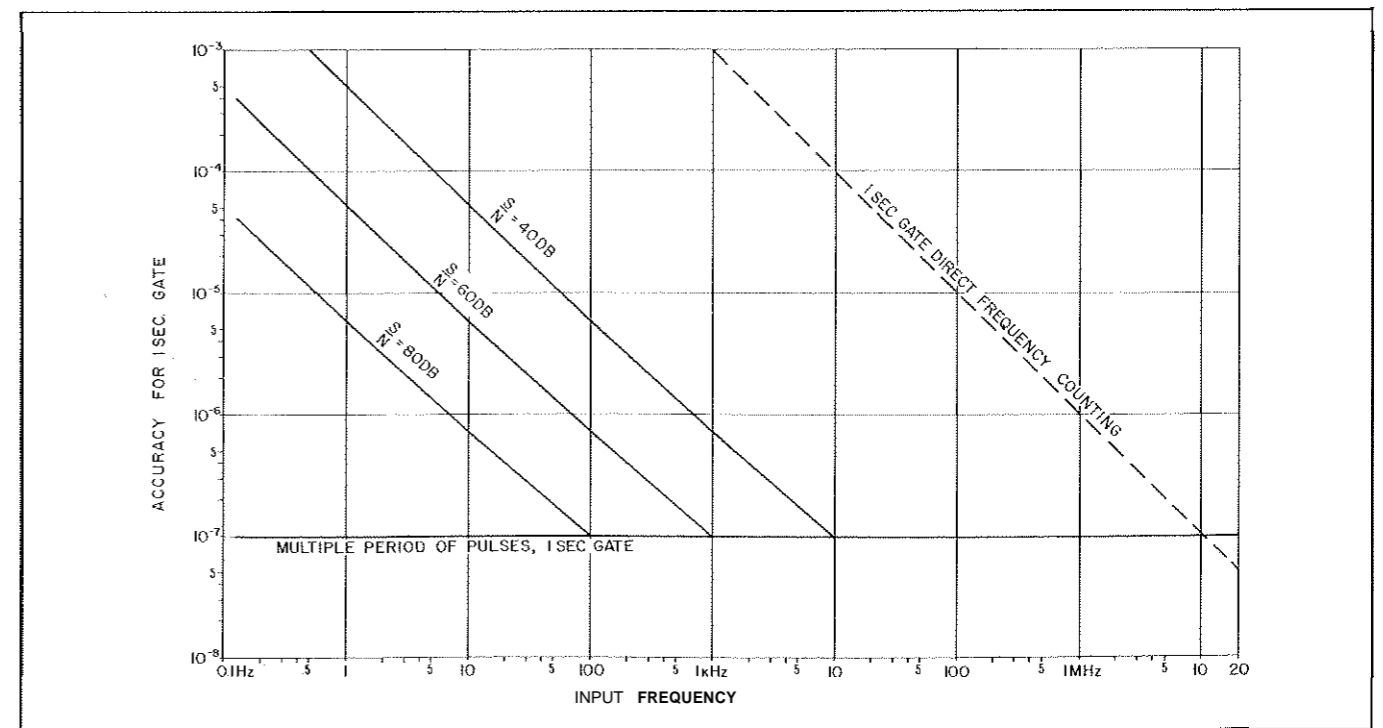
Measurement Time Setting	Most Significant Digit (MSD) of Input Frequency	
	MSD = 1 or Blank	MSD = 2 through 9
	Digits Displayed	Digits Displayed
.01	6	5
.04	6	5
.1	7	6
.2	7	6
.4	7	7
1	7	7
2	7	7
4	7	7

3-6. When a full input cycle does not occur during two times the selected measurement time, the Counter displays all zeros.

#### 3-7. ACCURACY

3-8. Accuracy of the 5323A is shown in Figure 3-1; accuracy for a conventional counter is shown for comparison. The accuracy shown in Figure 3-1 does not

Figure 3-1. Accuracy Versus Frequency



include time base errors (as an external time base could be used), but consists of a  $\pm 100$  nsec clock pulse ambiguity and a  $\pm$  trigger error for 100 mV sine wave input. With the LEVEL control set to PRESET, the error curves have a 99% confidence level.

3-9. Measurement resolution is limited only by  $\pm 1$  count of the 10 MHz time base, or  $\pm 100$  nsec time interval error. When MEASUREMENT TIME is decreased, resolution will degrade. For example:

Using a 1 second measurement time, the resolution is 1 sec/100 nsec, or 1 part in  $10^7$ , and all seven displayed digits are significant. Using a 0.1 second measurement time the resolution is 0.1 sec/100 nsec, or 1 part in  $10^6$ , and the last digit of 1000000 is significant; however, a readout of 9999999 would only be accurate to 110, and the last digit is blanked.

### 3-10. HYSTERESIS

3-11. The range selection circuits have a hysteresis control designed to reduce confusion when the

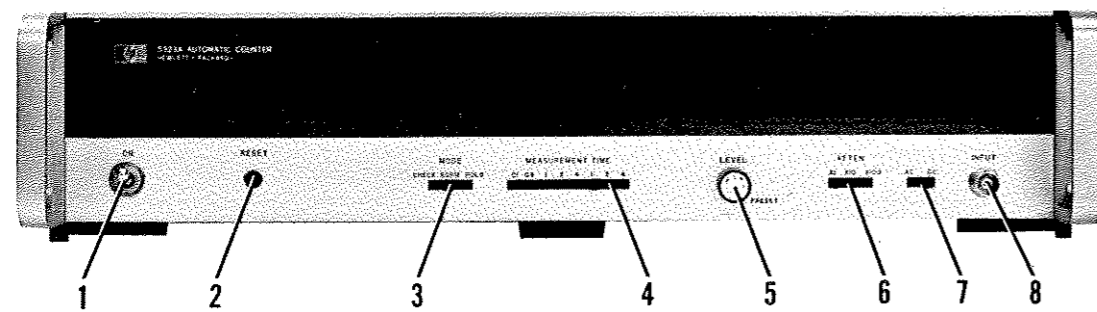
measured signal frequency is decreasing or changing about a decade value. For example:

With the Hysteresis switch on, if an input frequency of 999.9999 Hz increases 1 count to 1.000000 kHz, the range and decimal point change. However, if frequency decreases from 1.000000 kHz, the range and decimal point will remain unchanged until the frequency is  $< 0.900000$  kHz, then changes to 899.9999 Hz. This 10% hysteresis prevents unnecessary and confusing range changes.

### 3-12. RPM MEASUREMENTS

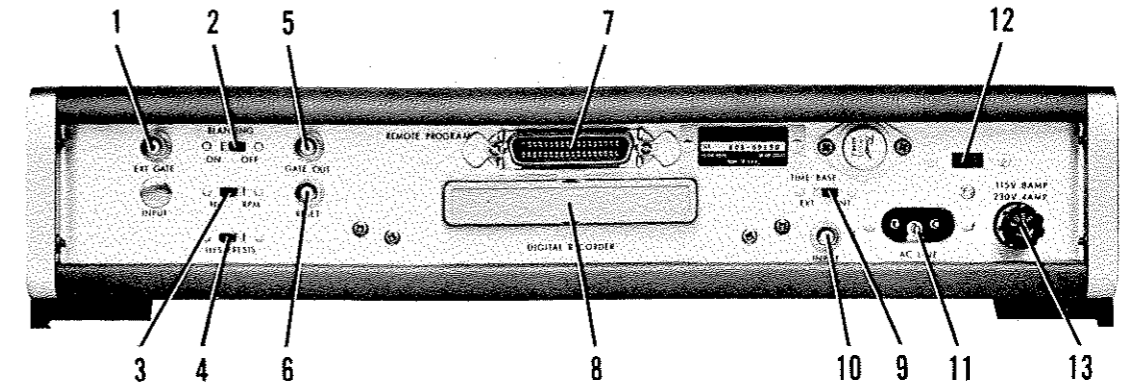
3-13. The Counter will measure RPM directly when the Hz/RPM switch is set to RPM. In this position, the internal 10 MHz clock is divided by 6, and the display decimal point is shifted one place, giving the effect of multiplying the input by 60. This will also increase the MEASUREMENT TIME by 6.

Figure 3-2. Front Operating Controls



1. POWER switch controls power to all circuits except part of Oscillator/Multiplier Assembly, (controlled by rear panel TIME BASE switch).
2. RESET pushbutton returns displayed and internal count to zero.
3. MODE:
  - a. Applies 10 MHz internal clock to Gate Board in CHECK position. Display will be 10.00000 MHz or 100.0000 RPM.
  - b. Permits frequency measurements of signals applied to INPUT connector in NORM position.
  - c. Prevents display from automatically re-setting in HOLD position.
4. MEASUREMENT TIME switch permits measurement time selections of .01, .04, .1, .2, .4, 1, 2, or 4 seconds.
5. LEVEL control selects input trigger level (multiplied by ATTEN setting). Trigger will occur at 0V when set to PRESET.
6. ATTN switch attenuates input signal amplitude by factors of 1, 10, or 100 (maximum overload; 120 Vrms in position 1, 250 Vrms in position 10, 500 Vrms in position 100).
7. AC-DC switch provides coupling to input amplifier through .033  $\mu$ F (AC), or directly (DC).
8. INPUT, 0.125 Hz to 20 MHz

Figure 3-3. Rear Operating Controls

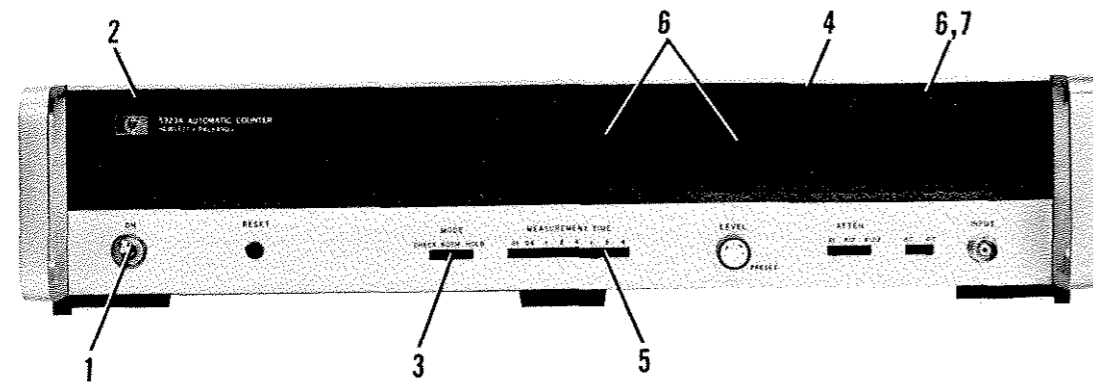


1. EXT GATE: permits use of an external gate signal for measurement times other than those on front panel (between 0 and 4 seconds).
2. BLANKING switch disables automatic blanking feature.
3. Hz-RPM switch converts display from frequency (Hz) to events-per-minute (RPM).
4. HYSTERESIS switch disables automatic hysteresis feature.
5. GATE OUT: provides 0V when Counter is counting (gate cycle) and +5V when not counting.
6. RESET: permits use of an external reset. Reset will occur when input is less than +0.8V.
7. REMOTE PROGRAM connector permits remote programming of:
  - a. RESET
  - b. SELF-CHECK
  - c. HOLD
  - d. BLANKING
  - e. HYSTERESIS
  - f. MEASUREMENT TIME
  - g. LEVEL
  - h. PRINTER HOLDOFF VOLTAGE
8. DIGITAL RECORDER connector supplies BCD information to recorder, digital-to-analog converter, or other data processing equipment.
9. TIME BASE switch selects either internal clock or permits use of an external time base. In INT position the internal clock is available as an output at connector J1, (10 MHz, 1.0V peak-to-peak).
10. J1 connector for applying external time base of 1, 2.5, 5, or 10 MHz, 1.0 Vrms (with TIME BASE in EXT) or counter's internal time base output (with TIME BASE in INT).
11. AC LINE connector connects with flat plug of power cable.
12. Line Voltage switch permits selection of 115V or 230V AC line; insert narrow-blade screwdriver and slide to left for 115V operation, slide to right for 230V operation.
13. Fuse provides overload protection; should be 0.8 ampere, slow-blow for 115V operation or 0.4 ampere, slow-blow for 230V operation.

#### CAUTION

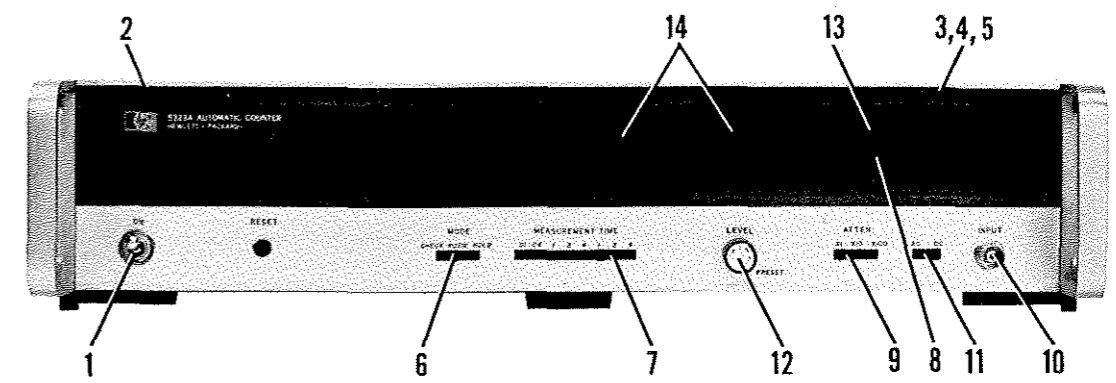
Before plugging instrument to AC power line be sure slide switch is properly positioned and correct fuse is installed.

Figure 3-4. Self-Check



1. Set POWER switch to ON.
2. Set TIME BASE switch (rear panel) to INT.
3. Set MODE switch to CHECK.
4. Set BLANKING switch (rear panel) OFF.
5. Set MEASUREMENT TIME switch to any position
6. Set Hz/RPM switch (rear panel) to Hz. Display should be 10.00000 MHz.
7. Set Hz/RPM switch to RPM. Display should be 100.0000 RPM.

Figure 3-5. Frequency Measurement



1. Set POWER switch to ON.
2. Set TIME BASE switch (rear panel) to INT.
3. Set BLANKING switch (rear panel) to ON.
4. Set Hz/RPM switch (rear panel) to Hz.
5. Set HYSTERESIS switch (rear panel) to ON.
6. Set MODE switch to CHECK to verify proper Counter operation (see Figure 3-4). Return MODE switch to NORM.
7. Set the MEASUREMENT TIME switch to the desired measurement time.
8. With no input signal, the ARM lamp should be illuminated.
9. Set ATTEN switch to X100.
10. Connect unknown signal to INPUT jack.
11. Set AC-DC switch to AC (10 Hz to 20 MHz) or DC (0.125 Hz to 20 MHz).
12. Adjust LEVEL control for a steady display. If there is no count, or if count is uncertain, switch ATTEN to a lower factor and readjust LEVEL control. Normally, the PRESET position will provide a steady display, with no DC offset voltage on the input signal.
13. The COUNTING lamp will illuminate, and the ARM lamp will go off when the measurement is being made.
14. Read frequency from display. Decimal point is correctly positioned, and correct measurement unit (MHz, kHz, or Hz) is displayed.

## SECTION IV THEORY OF OPERATION

### 4-1. INTRODUCTION

4-2. This section discusses the operation of individual circuits. Assemblies that make up the instrument are covered in detail in Section VIII, opposite each schematic diagram. Compute and Display Cycle timing, arithmetic operation, and overall Block Diagram are also described in this section.

### 4-3. Logic Symbols

4-4. Two states exist in the binary system, 1 and 0. HIGH (H) and LOW (L) are used to represent the levels of 1 and 0. HIGH always represents the more positive level, whether it be positive or negative logic. Figure 4-1 shows four pairs of logic symbols that have the same truth tables and can be used interchangeably. The same function is performed by what appears to be two different logic symbols.

4-5. GATES. Figure 4-2(A) represents a basic AND gate. The AND gate output is HIGH if all inputs are HIGH. An AND gate may have two or more inputs. Figure 4-2(B) represents a basic OR gate. The OR gate output is HIGH if one or more of its inputs is HIGH. An OR gate may have two or more inputs.

4-6. INVERSION. AND and OR gates are shown in Figure 4-2 (A, B). A circle on the output of a logic symbol indicates a LOW when activated as shown in Figure 4-2 (C and D). Thus, a circle indicates inversion. An AND gate with an inverted output is called a NAND gate; an OR gate with an inverted output is called a NOR gate. A unity-gain amplifier with an inverted output is called an inverter, Figure 4-2 (E).

Figure 4-2. Gate Symbols

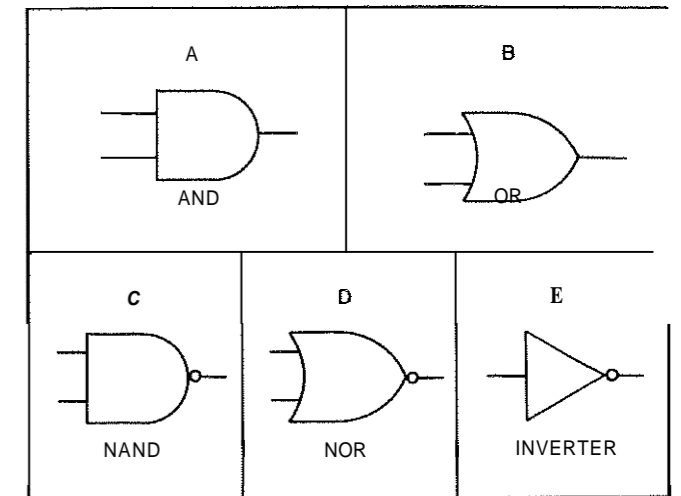
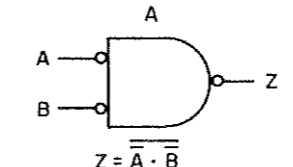
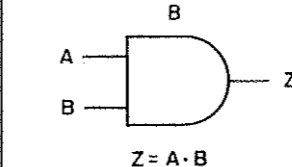
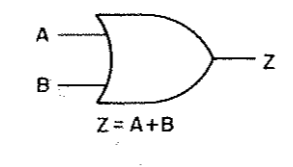
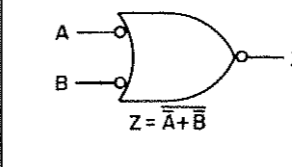


Figure 4-1. Logic Function Comparison

A			B			C			D		
 $Z = A \cdot B$			 $Z = \overline{A \cdot B}$			 $Z = A + B$			 $Z = \overline{A + B}$		
A	B	Z	A	B	Z	A	B	Z	A	B	Z
L	L	L	L	L	L	L	L	H	L	L	H
L	H	H	L	H	L	L	H	L	L	H	H
H	L	H	H	L	L	H	L	L	H	L	H
H	H	H	H	H	H	H	H	L	H	H	L

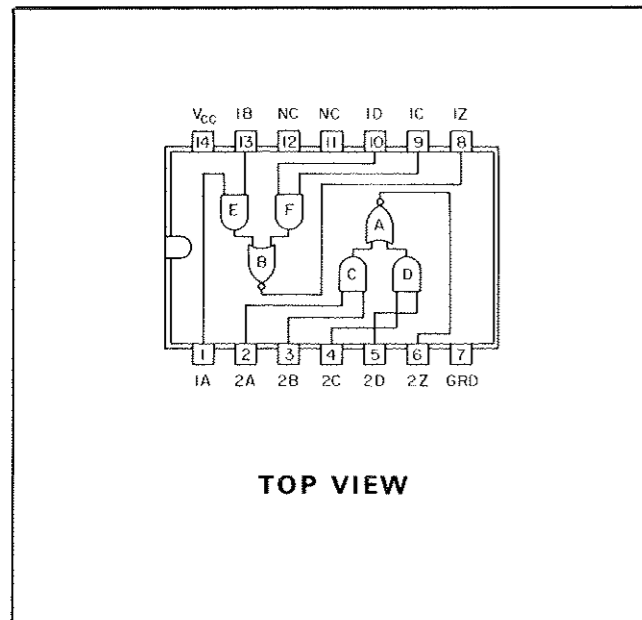
4-7. INTEGRATED CIRCUIT OPERATION

4-8. AND/OR Invert Gate

4-9. The DUAL AND/OR Invert Gate package is shown in Figure 4-3. The output (Z) will be LOW under three conditions:

- a. Inputs A and B are both HIGH, or
- b. Inputs C and D are both HIGH, or
- c. Inputs A, B, C, and D are all HIGH. At all other times, Z will be HIGH.

Figure 4-3. AND-OR Invert Gate (1820-0063)



TOP VIEW

Figure 4-4. Dual D Triggered Flip/Flop (1820-0077)

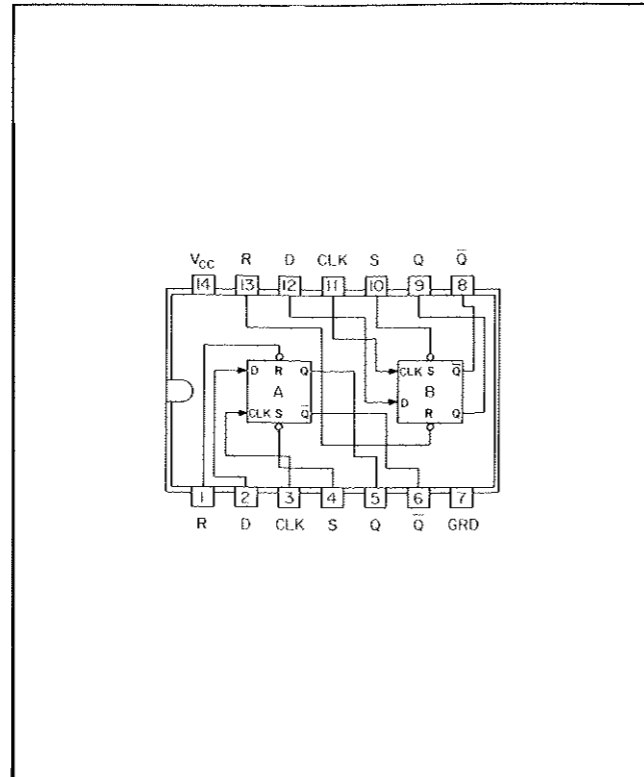
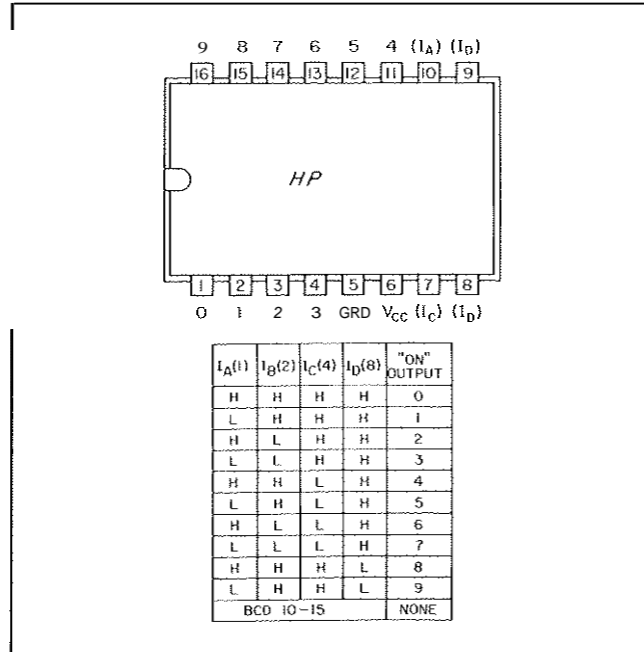


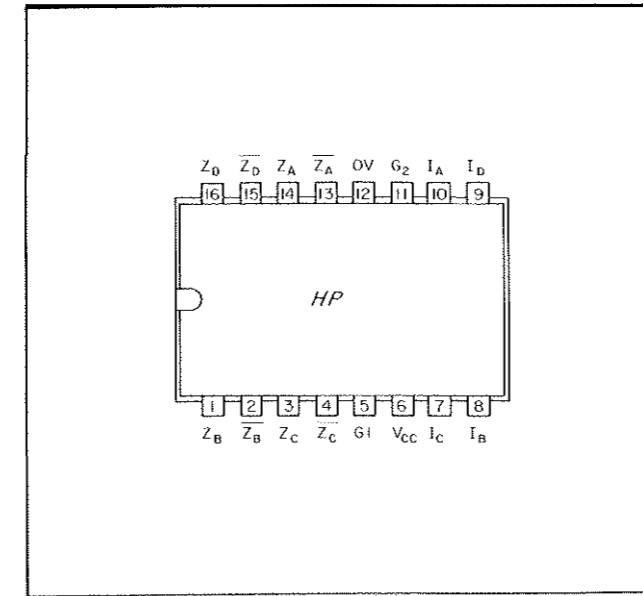
Figure 4-5. BCD to Decimal Decoder/Driver (1820-0092)



4-14. Four-Bit Buffer Storage

4-15. The 4-bit Buffer Storage package is shown in Figure 4-6. The 4-bit BCD input will be gated into the buffer when the G1 input is enabled by a LOW or open. The non-inverted output (Za, Zb, Zc, Zd) is in-phase with the input when G1 is LOW or open. The inverted output (Za-bar, Zb-bar, Zc-bar, Zd-bar) is enabled when G2 is HIGH. When G2 is LOW, the inverted output is HHHH.

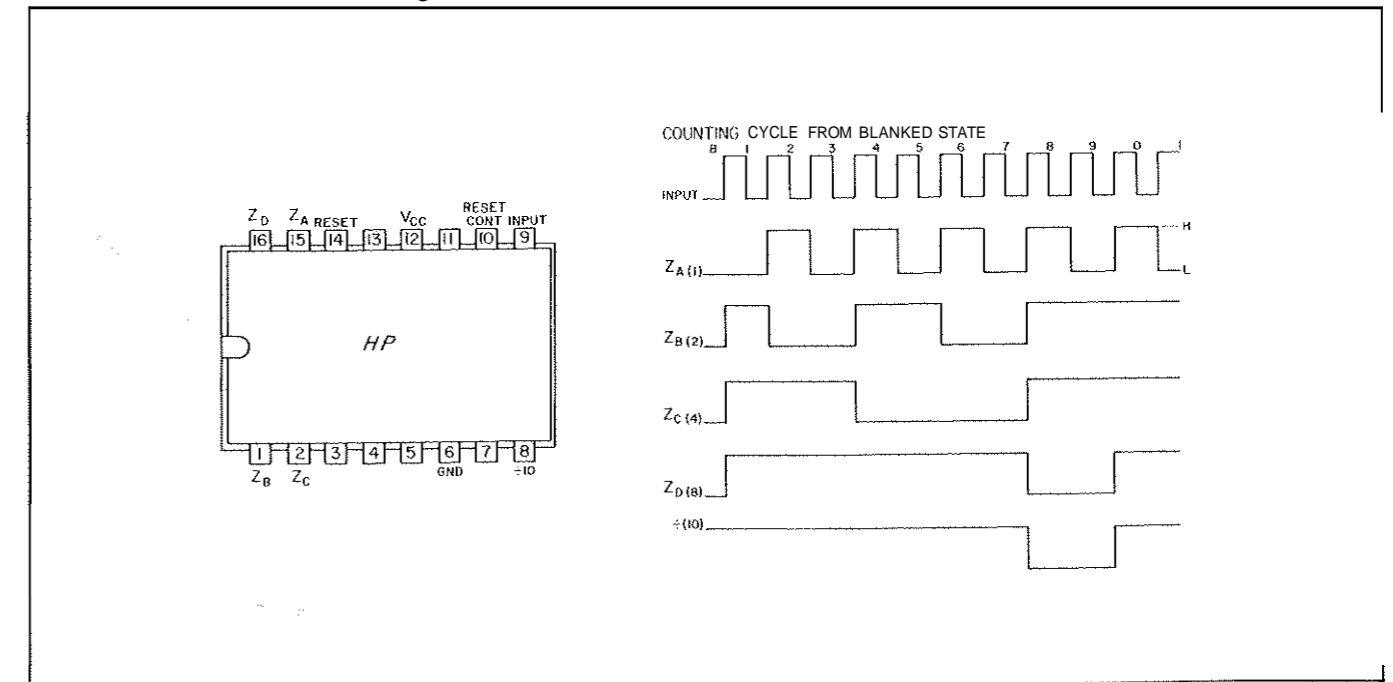
Figure 4-6. 4 Bit Buffer Storage (1820-0116)



4-16. Blanking Decade Counter

4-11. The Blanking Decade Counter package is shown in Figure 4-7. The counter has two reset states determined by the reset control input. If the reset control is LOW, a HIGH reset pulse will set the counter to LLLL (Blank). If the reset control is HIGH, a HIGH reset pulse will set the counter to HHHH (zero). The negative logic outputs are shown on the timing diagram.

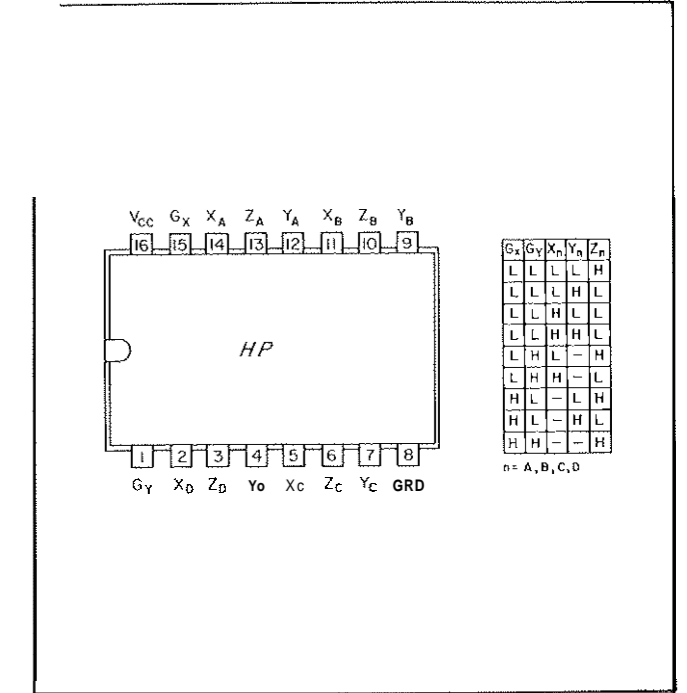
Figure 4-7. Blanking Decade Counter (1820-0119)



4-18. Four-Pole Switch

4-19. The 4-Pole Switch package is shown in Figure 4-8. The dashes in the input columns indicate that the state may be either HIGH or LOW without affecting the output (Z). Gx enables X inputs, Gy enables Y inputs.

Figure 4-8. 4 Pole Switch (1820-0135)



4-20. Decade Counter and Shift Register

4-21. The Decade Counter and Shift Register package is shown in Figure 4-9. The device operates either as a counter or as a shift register as shown in the timing diagram. A HIGH reset input will set all outputs HIGH. Both input and output use negative logic. The shift input should be HIGH when counting or re-setting. The maximum counting frequency of the 1820-0190 is 10 MHz and the 1820-0191 is 2 MHz.

Figure 4-9. Decade Counter and Shift Register (1820-0090/91)

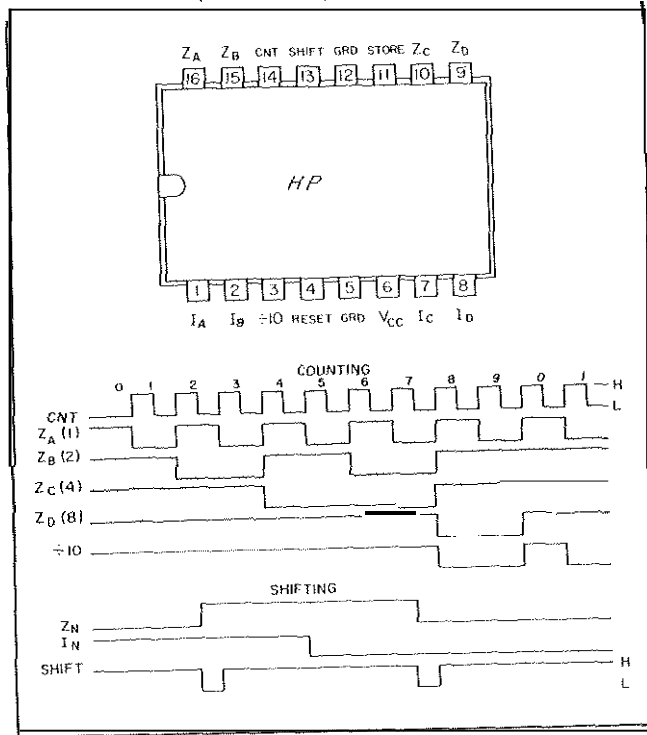
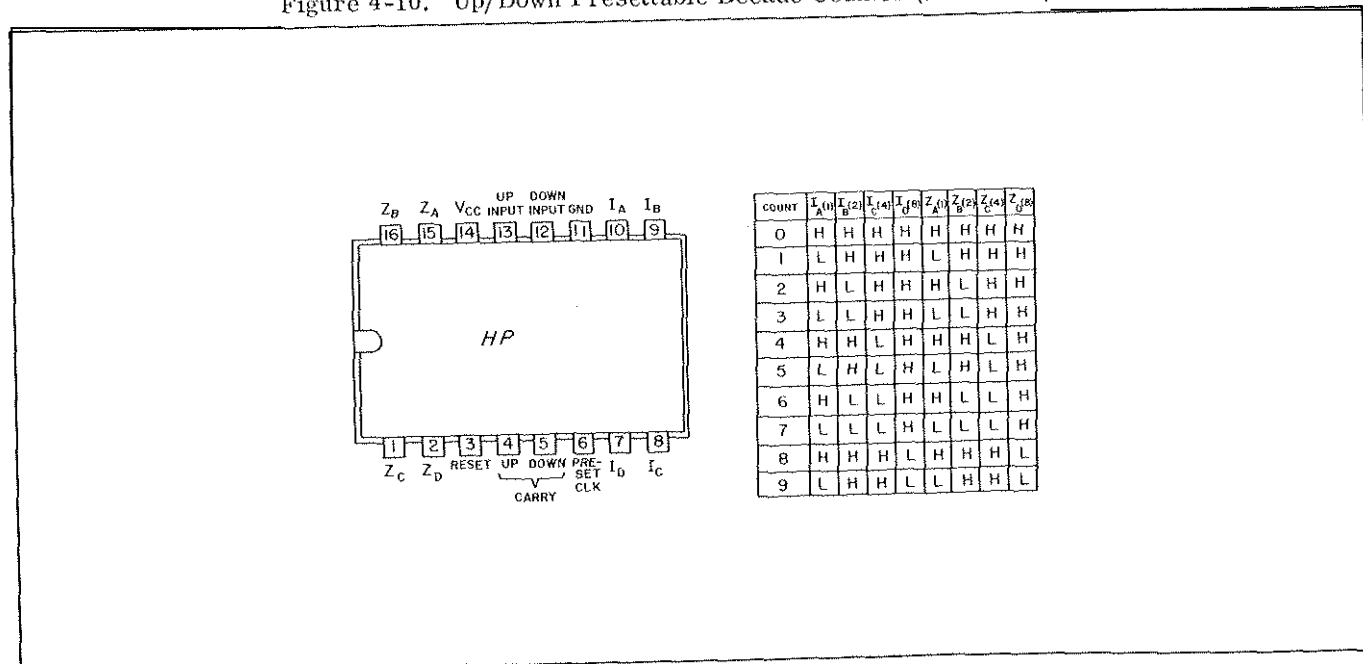


Figure 4-10. Up/Down Presettable Decade Counter (1820-0176)



4-22. Up/Down Presettable Decade Counter

4-23. The Up/Down Presettable Decade Counter package is shown in Figure 4-10. A number between 0 to 9 may be preset and then the decade will count either up or down from this value. The preset count will be set according to the truth table when the preset input goes HIGH. The up and down count inputs should be inhibited by a HIGH when enabling preset. The decade can be reset to zero by applying a HIGH to the reset input while the up and down count inputs are HIGH (inhibited). A LOW input to a count input will change the state of the decade (up or down); the unused count input must be inhibited by a HIGH.

4-24. J-K Flip/Flop

4-25. The dual J-K Master-Slave Flip/Flop package is shown in Figure 4-11. When both inputs are LOW, the clock has no effect. When the J input is HIGH, the positive clock transition will set Q HIGH. When the K input is HIGH, the positive clock transition will cause Q to go HIGH. When both inputs are HIGH, the flip/flop will change state (toggle) with each positive transition of the clock input. A LOW R input will override other inputs and reset the Q output LOW. The Q and Q outputs are always opposite in level.

4-26. Divide by 16 Counter

4-27. The Divide by 16 Counter package is shown in Figure 4-12, and is a 4-bit binary ripple counter. The negative logic 4-bit BCD outputs and the ÷16 output are shown in the timing diagram. A reset signal (HIGH) sets the outputs HIGH. The counter will advance on the leading edge of the input pulse.

Figure 4-11. Dual J-K Flip/Flop (1820-0208)

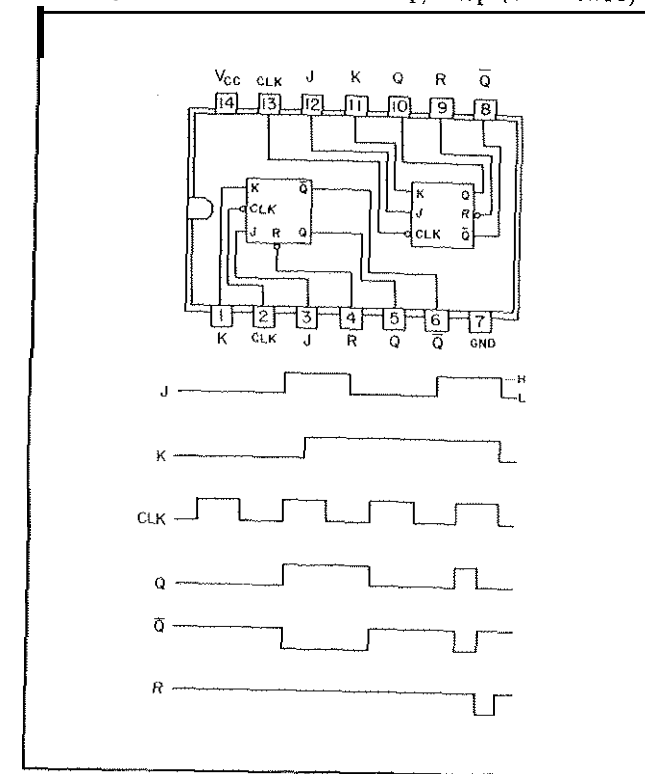
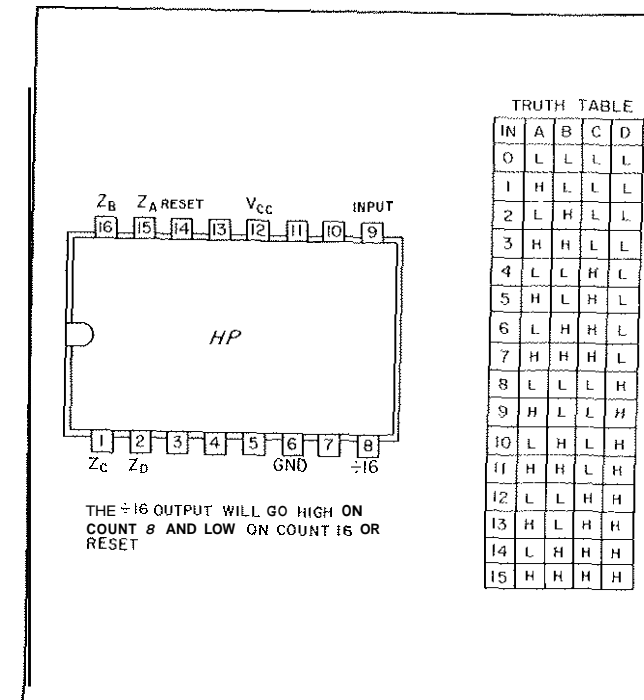


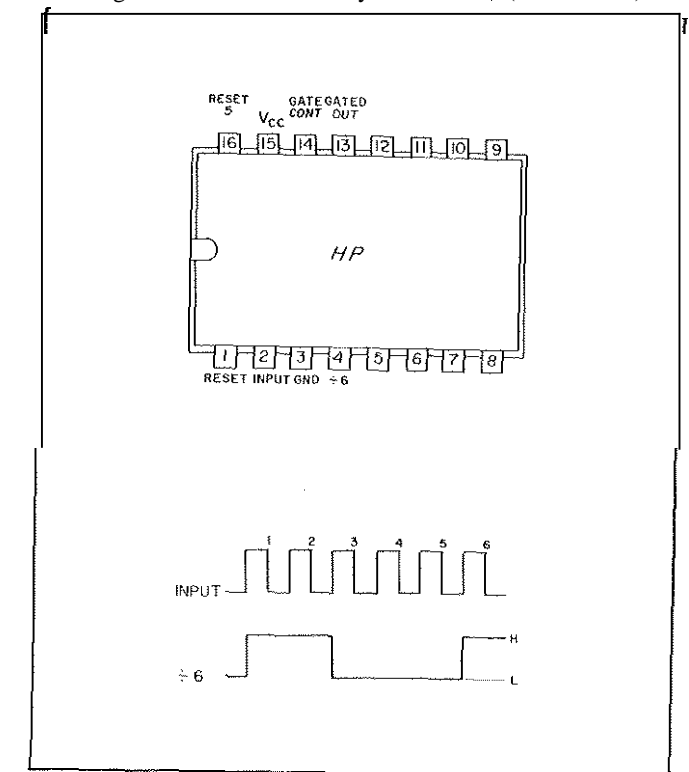
Figure 4-12. Divide by 16 Counter (1820-0209)



4-28. Divide by 6 Counter

4-29. The Divide by 6 Counter package is shown in Figure 4-13. The Gate Control input must be LOW to enable the gated output. The reset "0" or reset "5" inputs must be HIGH to enable the reset. The counter will advance on the leading edge of the input pulse.

Figure 4-13. Divide by 6 Counter (1820-0210)



4-30. Four-Bit Binary Full Adder

4-31. The 4-Bit Binary Full Adder package is shown in Figure 4-14, with its truth table. The adder adds two 4-bit binary numbers (A1, A2, A3, A4, and B1, B2, B3, B4) and a carry-in (C<sub>in</sub>) to produce their sum (Σ1, Σ2, Σ3, Σ4) and a carry-out (C4). The inputs A1, A2, B1, B2, and C<sub>in</sub> determine Σ1, Σ2, and the internal carry (C2). The inputs A3, A4, B3, B4, and internal carry C2 determine Σ3, Σ4, and C4.

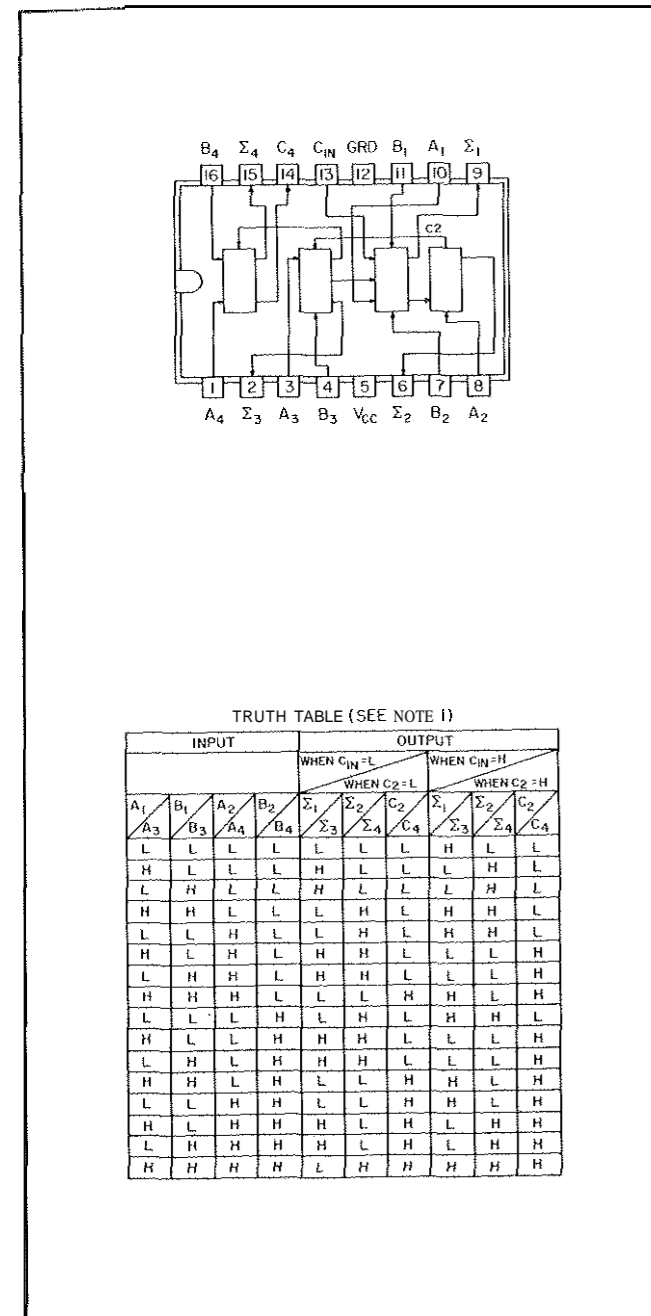
4-32. THEORY OF OPERATION

4-33. The operation of the HP 5323A is divided into three cycles: Gate, Compute, and Display. A flow diagram included in Section VIII (Figure 8-2) depicts the three cycles and the MEASUREMENT TIME process. A block diagram included in Section VIII (Figure 8-3) shows the functional relationship of the major assemblies and critical signals used by the assemblies. These figures should be folded out for reference during the following discussion.

4-34. Gate Cycle

4-35. Input frequency (F<sub>x</sub>) connects to A2 (Amplifier/Trigger) via A1 (Attenuator). The input signal triggers A2 and the narrow pulse produced, goes to A3. This pulse appears at the input of the F<sub>x</sub>/2 flip/flop, when MODE is set to NOIM. When MODE is set to CHECK, internal clock pulses (F<sub>y</sub> or F<sub>y</sub>/G) will appear at the F<sub>x</sub>/2 flip/flop instead of F<sub>x</sub>.

Figure 4-14. Four-Bit Binary Full Adder (1820-0305)



4-36 The first F<sub>x</sub> pulse will set the  $\frac{F_x}{2}$  flip/flop to Q HIGH, enabling the Single Cycle Register and the X-Gate Enable flip/flop, producing the GATE signal. GATE resets the 11-Register to D=15 signaling start of the Gate cycle. The COUNTING lamp will be on. The EXT GATE signal must be high to initiate the GATE signal.

4-37. The clock pulse from A14 (Oscillator/Multiplier) enables the Gate Control flip/flop enabling the Y-Gate. Y-Gate output is a series of COUNTY Y pulses, which are accumulated in the Y-Register. The clock frequency is 10 MHz. COUNTY Y pulses will be 10 MHz when the Hz/RPM switch is in Hz, or 10/6 MHz when in RPM.

4-38. The next F<sub>x</sub> pulse enables the X-Gate, and a COUNT X pulse will occur. COUNT X pulses continue at the  $\frac{F_x}{2}$  frequency and are accumulated in the X-Register. When the Y-Register contents equals the selected measurement time, a TIME signal occurs enabling the Single Cycle Register and X-Gate Enable flip/flop. The X and Y-Gates will be disabled by the next input pulse, terminating COUNT X and COUNT Y pulses and the GATE signal will return to its initial state.

4-39. When the input frequency period is longer than the selected measurement time, the Gate Control uses the Single Cycle Register to terminate the Gate Cycle on the second positive slope zero-crossing of the input. A PRESCALE signal is sensed by A7 (Control Board), which alters the Compute Cycle to correct for single-cycle operation.

4-40. Notice that clock and input frequencies are synchronized by the  $\frac{F_x}{2}$  flip/flop so that maximum error during the Gate cycle is equal to one clock period (100 nsec for Hz or 600 nsec for RPM). The selected measurement time is (T). At the end of the Gate Cycle Y-Register contains F<sub>y</sub> X T (or  $\frac{F_y}{F_x} X T$  for RPM) and X-Register contains F<sub>x</sub> X T. The X and Y-Registers contain information needed to calculate frequency F. When no input signal occurs after the TIME signal, a low-frequency reset signal occurs at 2 x Measurement Time.

**4-41. Compute Cycle**

4-42. Frequency (F) is calculated by dividing X-Register contents by Y-Register contents and multiplying the result by the clock frequency (F<sub>0</sub>), (F =  $\frac{X}{Y} \times F_0$ ). F is calculated one digit at a time. As each digit is calculated, it is transferred to the Display; decimal point position and measurement units for the Display are determined by the magnitude of X and Y. F calculation is performed by A5 (Adder Board) and A7, refer to Figures 4-15 and 4-17.

4-43. To divide X by Y, a process of repeatedly subtracting Y from X is used. To subtract Y from X, a technique known as nines complementing is used. The nines complement of X is the difference between each digit of X and the number 9. Sequentially, the nines complement of X (called X<sub>c</sub>) is added to Y; Y is then added to X until a left-digit carry occurs; the last sum (without the carry) is then complemented and added to Y to restore the remainder. The last step is required because Y must be added to X until a carry occurs, which is one step too far in the division process. The restored remainder is then multiplied by 10, and the process repeated to determine the next digit of F. The number of times that Y was added to X before a carry occurs is the value of the first digit of F (called Z). Figure 4-16 is an example of the arithmetic operations performed by A5; the first digit of F is 3.

Figure 4-15. Timing and Control Diagram

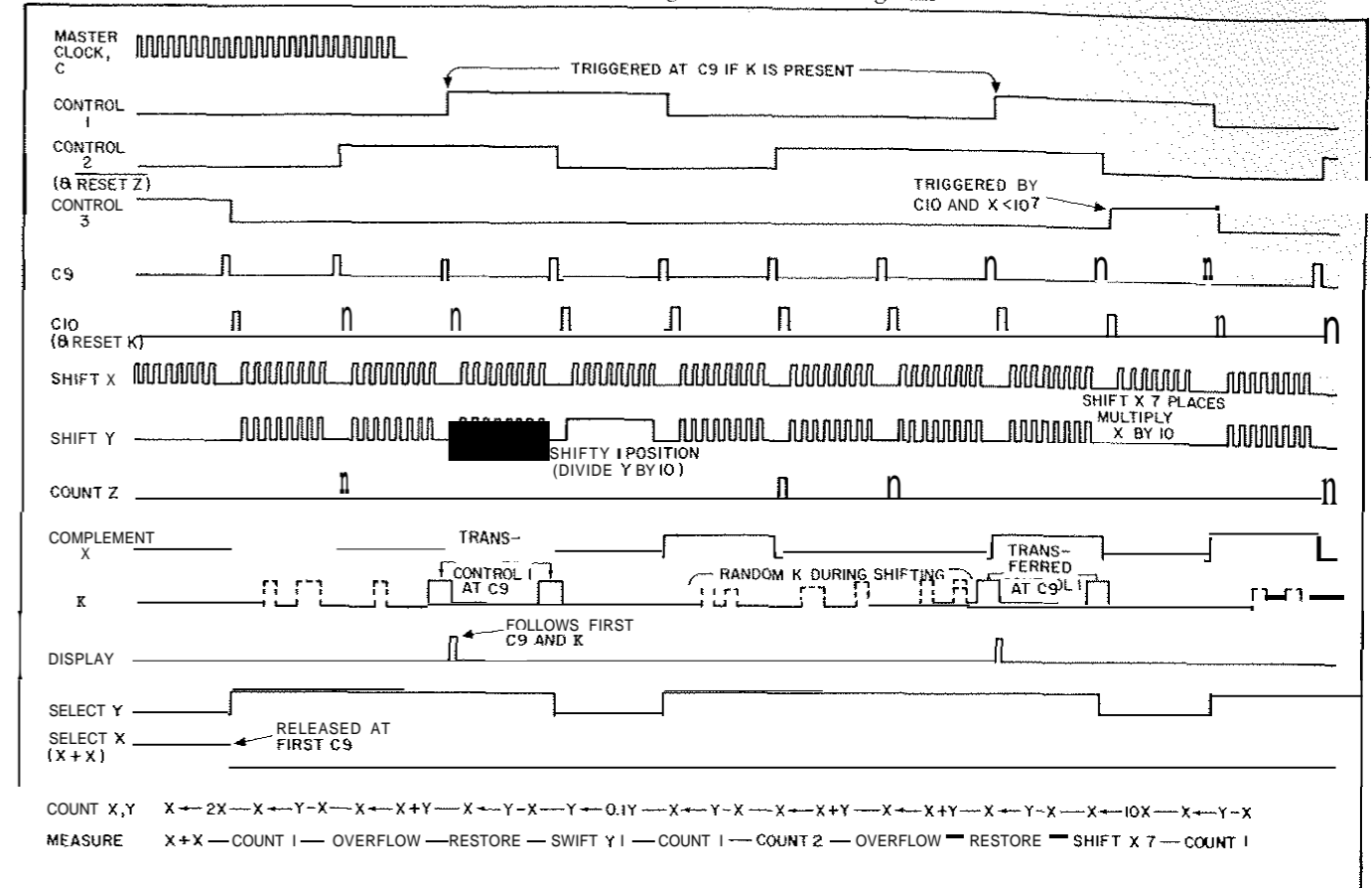
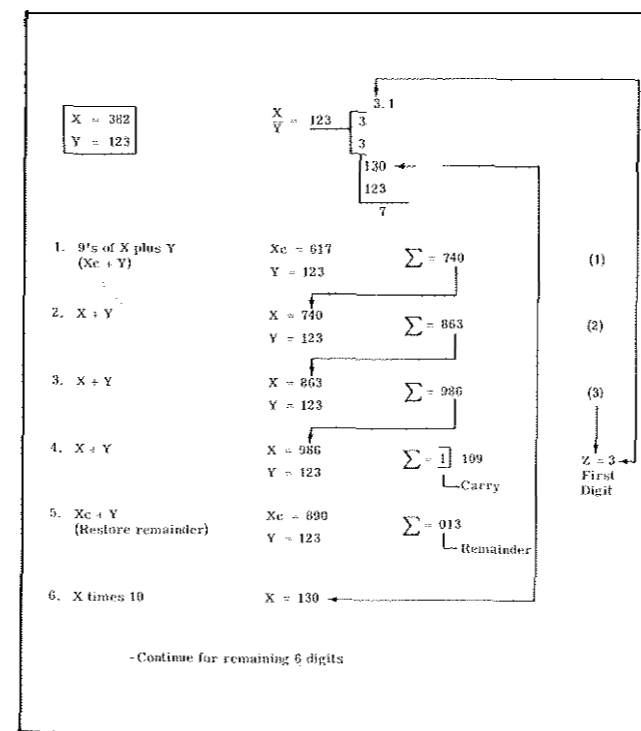


Figure 4-16. Arithmetic Operation



4-44. The first step in the calculation is to double the X-Register contents to correct for the division of the  $\frac{F_x}{2}$  flip/flop. A7 enables the 4-pole switches in A5, so that X + X occurs. When a single-cycle measurement occurs, X + X is inhibited because F was not divided by two (refer to Figure 4-15).

4-45. The next operation initiated is complementing X-Register contents and adding the results to the Y-Register contents (X<sub>c</sub> + Y). A7 then sets the 4-pole switches to perform an X + Y operation. The operation is repeated until a carry from the Adder occurs (equivalent to a negative remainder). The correct remainder is restored by using the X<sub>c</sub> + Y operation, because we have made one extra subtraction. The remainder is now multiplied by 10, and the second digit of F will be calculated. This process is repeated until all 7 digits of F have been determined. Note the Y-Register contents are recirculated during the compute cycle (Y remains unchanged).

4-46. Shift pulses for X and Y-Registers and control pulses for the 4-pole switches in A5 are generated by A7, using clock pulses. The carry pulses are used by the Control Board to generate COUNT Z and DISPLAY signals.

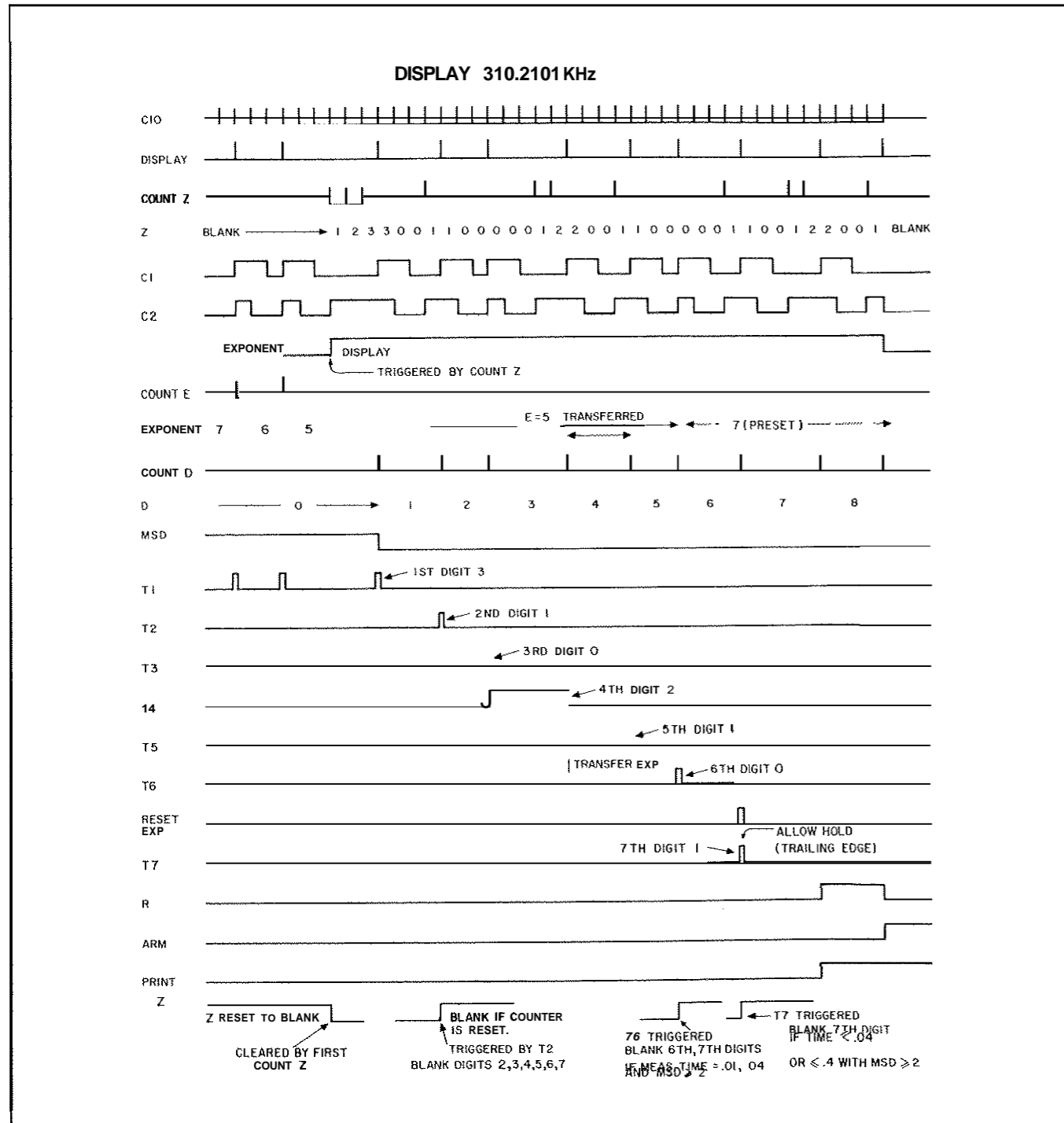


4-47. Display Cycle

4-48. The Compute and Display Cycles occur at the same time. As each digit of F is calculated it must be transferred to buffer storage and the Display. At the start of the Compute and Display Cycles, the GATE signal ending the Gate Cycle resets the D-Register to D = 0.

4-49. During the Compute Cycle, when the first division is attempted (first digit calculation) a carry may occur. Each time such a carry occurs, a DISPLAY pulse is generated by A7 (refer to Figure 4-17). These DISPLAY pulses increment either the E or D-Registers, depending on the state of the Range Detector. In case of an immediate carry during first digit calculation, the DISPLAY pulse would decrease the

Figure 4-17. Display 310.2101 kHz



E-Register count, and no COUNT D pulse would occur. DISPLAY pulses will continue to decrease the E-Register count until a successful subtraction occurs (no carry), and a COUNT Z pulse is produced by the Control Board. The initial COUNT Z pulse causes the Range Detector to disable the E-Register input and enable the D-Register input. The COUNT Z pulses are accumulated in the Z-Register and represent one digit of F.

4-50. When a carry occurs after successful subtraction, DISPLAY and COUNT D pulses are generated. The most significant digit (MSD) is now transferred from the Z-Register to the buffer storage and Display, and the D-Register advanced to D = 1. Each new DISPLAY pulse will produce a COUNT D pulse to advance the D-Register, until all 7 digits have been calculated and displayed. The last digit will be transferred at D = 6.

4-51. At D = 4, the contents of the Exponent Register are transferred to the decimal and measurement unit decode logic. The location of the decimal point and the measurement unit (MHz, kHz, or Hz) are determined and transferred to the Display and Annunciator. When the Hz/RPM switch is set to RPM, the clock frequency is divided by 6, and the E-Register is changed by one count (X10) resulting in multiplication by 60.

4-52. After the last digit has been calculated, DISPLAY pulses will continue to be generated by A7 and continue to advance the D-Register, unless a HOLD is present. If the MODE switch is set to HOLD at

this time, the Clock Gate in A3 will be disabled, inhibiting the DISPLAY and COUNT D signals to preserve the display. If no HOLD is present, or when it is removed, the D-Register will advance to D = 7. D = 7 is a blank state, but D = 8 causes the PRINT Command and R-bar signal to be generated. The R-bar signal is an automatic reset which clears the X, Y, and Z-Registers.

4-53. At D = 9, the ARM signal is generated, turning the ARM lamp on, resetting the Range Detector, inhibiting the clock in A7 and enabling the Gate Control in A3 for the next Gate Cycle.

4-54. When the BLANKING switch is ON, the Blanking Control logic will automatically blank the sixth and/or seventh display digit, if the selected measurement time is so short that false resolution would occur.

4-55. When the HYSTERESIS switch is OFF, and the first digit changes from 1 to 9 in successive measurements, the decimal point and display will shift, and the measurement unit may change. To prevent this condition, the hysteresis feature may be used. With the HYSTERESIS switch ON, the Hysteresis Control logic senses the state of the MSD < 2 Memory and Z-Register contents. When the first digit changes from 1 to 9, the first Display digit will be blanked, the E-Register will be advanced, and an extra COUNT D pulse will advance the D-Register to D = 1. The first digit (Z = 9) will be transferred to the second display position, and the remaining digits are calculated and displayed. Hysteresis is effective only for descending range changes.

## SECTION V MAINTENANCE

### 5-1. INTRODUCTION

5-2. This section gives maintenance and service information. Included is a table of recommended test equipment, disassembly and repair procedures, in-cabinet performance check which may be used to verify proper Counter operation, overall troubleshooting procedures, and adjustments. Theory of operation and specific troubleshooting information for each assembly are located in Section VIII, opposite each schematic diagram.

### 5-3. ASSEMBLY DESIGNATIONS

5-4. Table 5-1 lists the designations, name, and Hewlett-Packard part number of assemblies used in this instrument.

### 5-5. TEST EQUIPMENT

5-6. Test equipment recommended for maintaining and checking performance is listed in Table 5-2. Test equipment having equivalent characteristics may be substituted for the equipment listed.

### 5-7. ASSEMBLY CONNECTION IDENTIFICATION

5-8. Throughout the manual, connections to printed circuit assemblies are referred to in abbreviated form. For example, connection to A3, pin 10 is A3(10).

Table 5-1. Assembly Identification

Assy	Name	HP Part No.
A1	Attenuator Board	05323-60006
A2	Input Amplifier Board	05325-60035
A3	Gate and Reset Board	05323-60011
A4	X-Register Board	05323-60005
A5	Adder Board	05323-60002
A6	Y-Register Board	05323-60003
A7	Control Board	05323-60004
A8	Display Control Board	05323-60009
A9	Connector Board	05323-60014
A10	Function Switch	05323-60007
A11	Main Board	05323-60001
A12	Display Board	05323-60008
A13	Annunciator Board	05323-60017
A14	Oscillator/Multiplier Board	05325-60008
A15	Crystal/Oven 10 MHz	05325-60012
A16	+5.1V and +175V Supply	05325-60022
A17	±12V Supply	05325-60005

### 5-9. IN-CABINET PERFORMANCE CHECK

5-10. GENERAL. The performance check, Table 5-3, and test card can be used to verify proper operation of all circuits in the Counter and may also be used:

- As part of an incoming inspection check of instrument specifications.
- Periodically, for instruments used in systems where maximum reliability is important.
- As part of a procedure to locate defective circuits.
- After any repairs or adjustments, and before returning instrument to regular service.
- As a permanent record of instrument maintenance performed, because the test record pages are perforated and may be removed.

5-11. VARIABLE LINE VOLTAGE. During the test (Table 5-3), Counter should be connected to a variable voltage source so the line voltage may be varied  $\pm 10\%$  from nominal (115 or 230 Vac).

### 5-12. INSTRUMENT COVER REMOVAL

5-13. To remove top or bottom cover, remove the four screws which secure cover to instrument. Slide cover toward rear of instrument and lift off. To replace cover, reverse procedure.

#### WARNING

115/230 VAC AND +175 VDC SUPPLY WIRES ARE EXPOSED WHEN EITHER TOP OR BOTTOM COVER IS REMOVED. USE EXTREME CAUTION DURING TROUBLESHOOTING, ADJUSTMENT, OR REPAIR. AVOID DAMAGE TO INSTRUMENT BY REMOVING POWER BEFORE REMOVING OR REPLACING COVERS, ASSEMBLIES, OR COMPONENTS.

### 5-14. ASSEMBLY LOCATION

5-15 Top internal, front and rear panel views of the Counter are shown in Figure 5-1. This figure shows the location of the assemblies, connectors, and chassis parts.

Figure 5-1. Top Internal, Front and Rear Panels

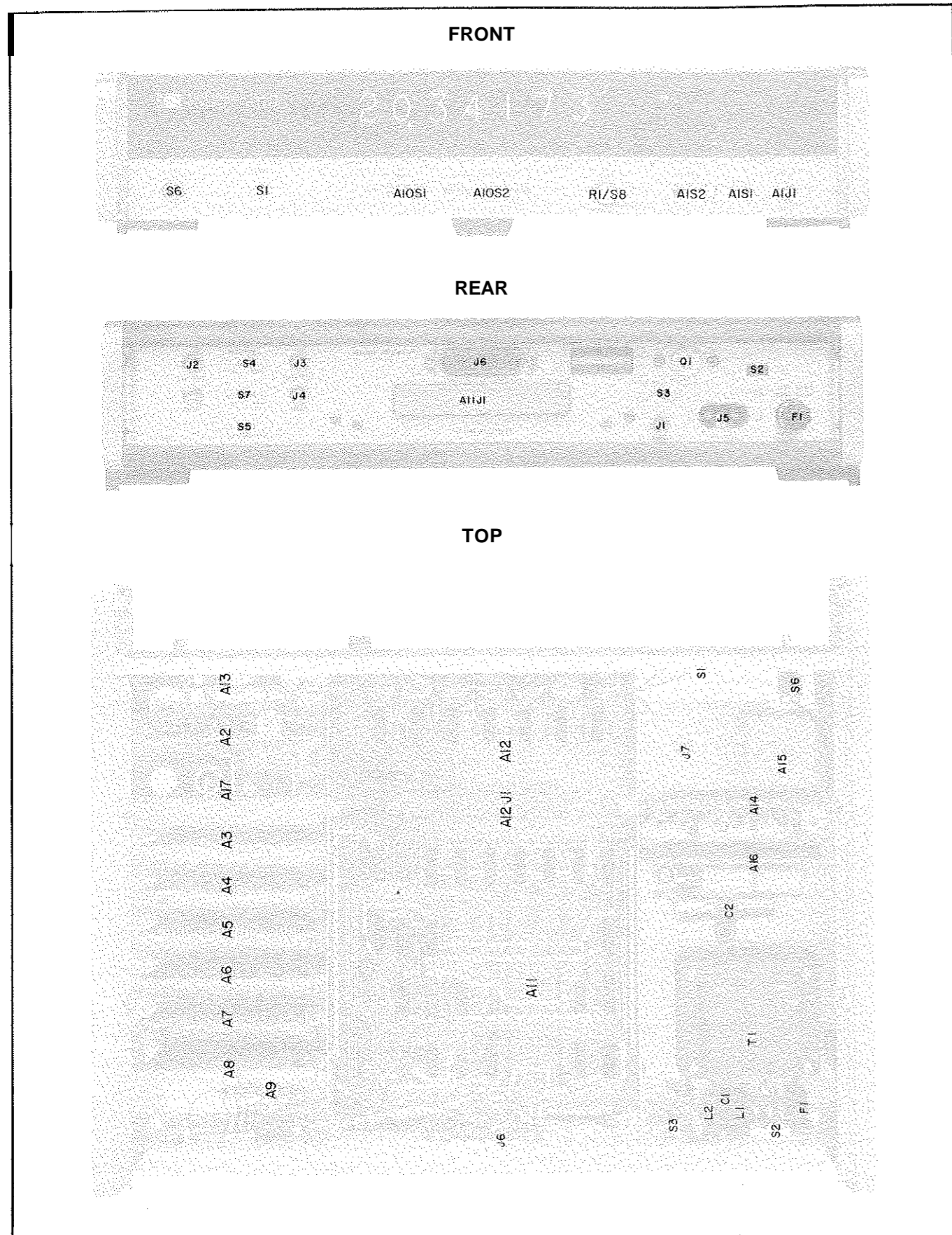


Table 5-2. Recommended Test Equipment

Instrument Type	Required Characteristics	Recommended Type
Oscilloscope	50 MHz Bandwidth, plug-in capabilities	HP 180A
Vertical Plug-in	50 mV/cm sensitivity, 50 MHz Bandwidth	HP 1801A
Time Base Plug-in	50 nsec/cm sensitivity	HP 1820A
Frequency Synthesizer	50 Hz to 20 MHz, 100 mVrms	HP 5100B
Synthesizer Driver	1 MHz output, 1.0 Vrms	HP 5110B
Digital Recorder	Compatible with BCD weighting used	HP 5050B
50Ω Feed-Thru Termination		HP 10100A
Cable Assembly	Compatible with Digital Recorder/Counter	HP 10524A
Low-Frequency Function Generator	0.1 Hz to 1100 Hz, 1V peak-to-peak, ±2%	HP 202A
Variable Attenuator	12 dB in 1 dB steps	HP 355C
Variable Attenuator	120 dB in 10 dB steps	HP 355D
Pulse Generator	30 nsec, ±0.3V, 10 MHz	HP 222A
RF Voltmeter	10 mV to 10V, 20 MHz, ±3% FS	HP 411A
DC Volt-Ohm-Ammeter	0 to +10V, ±1%, R x 1 capability	HP 412A
BNC "T" Connector		HP Part No. 1250-0781
Variable Line Voltage Source	Variable from 103 to 127 Vac (207 to 253 Vac)	
VIIF Oscillator	20 MHz, 300 mVrms	HP 32000
Frequency Standard	1 MHz, stability < 2 parts in 10 <sup>11</sup> per month	HP5065A or HP5061A
Resistive Probe	10:1, 10 pF, DC to 20 MHz	HP 10003A
Electronic Counter	20 MHz, 8-digit readout	HP 5245M
Current Probe	10 mA to 50 mA, 1 mV/mA sensitivity	HP 1110A
DC Probe Amplifier	Compatible with probe used	HP 1111A
Logic Probe	Compatible with DTL and TTL voltage levels	HP 10525A
Resistive Probe	50:1, DC to 10 MHz	HP 10002A

**5-16. REMOVAL OF PRINTED CIRCUIT BOARDS**

5-11. MAIN BOARD (A11). To remove this board:

- a. Remove top cover (see paragraph 5-12).
- b. Remove the 10 wires which are connected to the top of the board by push-on connectors. Each terminal on the board is color-coded to the mating wire color.
- c. Remove the 7 screws that secure the board to the chassis and connector J4.
- d. Slide board toward rear of Counter until A11J2 is disengaged from the Display Board (A12).
- e. Raise the front of the board to clear the Display Board (A12) and slide the board forward until A11J1 is out of the rear panel slot. Remove the board from the unit.

f. When reinstalling the board, do not connect any wire to the terminal between IC15 and IC19 (see Section VIII). This is a special test point.

5-18. DISPLAY BOARD (A12)

- a. Remove the Main board (A11) (see paragraph 5-17).
- b. Remove printed circuit board A2, A17, A3, A4, A5, and A6.
- c. Remove Annunciator Board (A13) by removing two nuts and washers that secure the assembly to the front panel.
- d. Remove the WHT-RED wire which is connected to the Display Board by a push-on connector.
- e. Remove the 4 screws that secure the board to the chassis. Remove board from unit.

5-19. CONNECTOR BOARD (A9)

- a. Remove top and bottom covers (see paragraph 5-12).
- b. From top of Counter, remove 3 large screws attaching the Main Board (A11) to connector A9J4.
- c. From bottom of board, remove connectors attached to A9J2 and A9J3.

**CAUTION**

Take care not to put a strain on connecting wires or bend them too many times. This will cause the wires to break or become weakened.

- d. Unsolder the 7 wires and 2 coaxial cables connected to the front of the board

- e. From top of Counter, remove the 8 wires connected to the board by push-on connectors. These connectors are accessible through a cutout in the chassis, located behind the Display Control Board (A8). The A7 and A8 boards may be removed to provide more access to the connectors.

- f. From the bottom of the Counter, remove the 6 screws and spacers that secure the board to the chassis. Do not remove the 3 screws securing connector A9J4 to the board. Remove the board from the bottom of the Counter.

**5-20. REPAIR**

**5-21. Printed Circuit Component Replacement**

5-22. Component lead holes in the circuit boards have plated-through walls to ensure good electrical contact between conductors on opposite sides of the board. To prevent damage to the plating and the replacement component, apply heat sparingly, and work carefully.

**5-23. Replacing Integrated Circuits**

5-24. Following are two recommended methods of replacing integrated circuits:

- a. **SOLDER GOBBLER.** This is the best method. Solder is removed from board by a soldering iron with a hollow tip connected to a vacuum source.
- b. **CLIP-OUT.** This method should be used as a last resort only. Clip the leads as close to the case as possible. With a soldering iron and long nose pliers, carefully remove the wires from each hole. Then clean the holes.

**5-25. ADJUSTMENTS**

5-26. The adjustments in Table 5-4 are in the order they should be performed, but should not be done unless:

- a. A trouble has been repaired which would affect these values.
- h. The instrument does not meet all specifications while performing the check in Table 5-3 (In-Cabinet Performance Checks).

Table 5-3. In-Cabinet Performance Check

FREQUENCY/RPM MEASUREMENTS	
<b>1. SELF-CHECK</b>	
a. Set Counter controls as follows:	
MODE . . . . .	CHECK
MEASUREMENT TIME . . . . .	.4
TIME BASE . . . . .	INT
Hz/RPM . . . . .	Hz
b. Display should be 10.00000 MHz, and COUNTING lamp ON. Record on test card.	
<b>2. DECIMAL POINT/MEASUREMENT UNITS</b>	
a. Set Counter controls as follows:	
MODE . . . . .	NORM
MEASUREMENT TIME . . . . .	.4
LEVEL . . . . .	PRESET
ATTEN . . . . .	X1
AC-DC . . . . .	DC
BLANKING . . . . .	ON
Hz/RPM . . . . .	Hz
HYSTERESIS . . . . .	ON
TIME BASE . . . . .	EXT

Table 5-3. In-Cabinet Performance Check (Cont'd)

FREQUENCY/RPM MEASUREMENTS (Cont'd)	
b. Connect Frequency Synthesizer output to Counter INPUT through a 50-ohm feedthrough termination.	
c. Connect Synthesizer Driver 1 MHz output to Counter external time base INPUT (rear panel).	
d. Connect Digital Recorder to Counter DIGITAL RECORDER connector.	
<u>Note</u>	
Refer to Operating and Service Manual for Digital Recorder Installation and Operation Information.	
e. Set synthesizer frequency to the values in Table 5-3A. Decimal point location, measurement unit, and printed exponent are shown in Table 5-3A. Displayed and printed digit values (N) are disregarded during this test. Record display and printed exponent on test card.	

Table 5-3A. Decimal Point/Measurement Unit

Synthesizer Frequency	Display	Printed Exponent
10 MHz	NN. NNNNN MHz	7
1 MHz	N. NNNNNN MHz	6
100 kHz	NNN. NNNN kHz	5
10 kHz	NN. NNNNN kHz	4
1 kHz	N. NNNNNN kHz	3
100 Hz	NNN. NNNN Hz	2
50 Hz	NN. NNNNN Hz	1
0 Hz	0. Hz	0

**3. ACCURACY**

- a. Set synthesizer frequency to the values in Table 5-3B. Display should be within  $\pm 1$  count of the selected frequency. Record display value and printed value on test card; printed and displayed values should be identical. Disconnect Digital Recorder.

Table 5-3B. Accuracy

1. 111111 MHz
2. 222222 MHz
3. 333333 MHz
4. 444444 MHz
5. 555555 MHz
6. 666666 MHz
7. 777777 MHz
8. 888888 MHz
9. 999999 MHz

**4. HYSTERESIS**

- a. Set Counter controls as shown in step 2a.
- b. Set synthesizer frequency to 1.000000 MHz, then decrease to .9888888 MHz. Display should be .988888 MHz. Record on test card.
- c. Set HYSTERESIS to OFF. Display should be 988.8888 kHz. Record on test card.

Table 5-3. In-Cabinet Performance Check (Cont'd)

**FREQUENCY/RPM MEASUREMENTS (Cont'd)**

5. BLANKING

- a. Set Counter controls as shown in step 2a.
- b. Set synthesizer to 2 MHz.
- c. Set MEASUREMENT TIME as shown in Table 5-3C. The number of digits displayed is shown in Table 5-3C. Record on test card.
- d. Set synthesizer to 1 MHz and repeat step 4c.
- e. Set synthesizer to 9.88888 MHz and repeat step 4c.

Note

Change frequency from 10.00000 MHz to 9.88888 MHz to enable hysteresis circuits.

- f. Set synthesizer to 1 MHz. Set Counter BLANKING switch OFF and MEASUREMENT TIME switch to .01. Seven digits should be displayed. Record on test card.

Table 5-3C. Blanking Check

MEASUREMENT TIME	DISPLAYED DIGITS		
	2 MHz	1 MHz	0.88888 MHz
4	7	7	6
2	7	7	6
1	7	7	6
.4	7	7	6
.2	6	7	6
.1	6	7	6
.04	5	6	5
.01	5	6	5

6. RPM

- a. Set Counter controls as shown in step 2a, except set Hz/RPM to RPM and MEASUREMENT TIME to .1. Adjust synthesizer frequency to values in Table 5-3D. Record display value on test card.
- b. Disconnect synthesizer and synthesizer driver from Counter. Set Counter TIME BASE to INT.
- c. Connect Low Frequency Function Generator to Counter INPUT with BNC "T" connector. Connect oscilloscope vertical input to the "T" connector.
- d. Set function generator output for a 1V P-P, 10 Hz sine wave measured on oscilloscope.
- e. Display should be 600.000 RPM  $\pm 2\%$ . Record on test card.
- f. Set Function Generator Frequency to 1 Hz (1V P-P sine wave). Display should be 60.0000 RPM  $\pm 2\%$ . Record on test card.
- g. Set Function Generator Frequency to 0.1 Hz (1V P-P sine wave). Display should be 6.00000 RPM  $\pm 2\%$ . Record on test card.

Table 5-3D. RPM Display

FREQUENCY	DISPLAY
10 MHz	600.000 RPM
1 MHz	60.0000 RPM
100 kHz	6.00000 RPM
10 kHz	600000. RPM
1 kHz	60000.0 RPM
100 Hz	6000.00 RPM
0 Hz	0. RPM

Table 5-3. In-Cabinet Performance Check (Cont'd)

RESET AND HOLD

1. RESET

- a. Connect equipment as described in step 6c of Frequency/RPM Tests. Set function generator output for 1 kHz sine wave at 1V P-P.
- b. Set Counter controls as shown in step 2a of Frequency/RPM Tests, except set MEASUREMENT TIME to 1 and TIME BASE to INT.
- c. Depress and release the RESET pushbutton.
- d. Display should be zero for 1 second, then display 1 kHz  $\pm 2\%$ . Record on test card.
- e. Remove signal at Counter INPUT.
- f. Display should reset to zero after 1 to 2 seconds and ARMED lamp should illuminate. Record on test card.
- g. Re-connect signal to INPUT.
- h. COUNTING lamp should illuminate and display should be 1 kHz  $\pm 2\%$  after 1 second. Record on test card.

2. HOLD

- a. Set function generator frequency to 1.1 kHz sine wave at 1V P-P. Set MODE to HOLD and AC-DC to AC.
- b. The Display should be 1.1 kHz  $\pm 2\%$ . Record on test card.
- c. Depress and release RESET.
- d. Display should reset to zero for 1 second, then display 1.1 kHz  $\pm 2\%$ . Record on test card.

3. LOW-FREQUENCY RESET

- a. Set MODE to NORM and AC-DC to DC.
- b. Set MEASUREMENT TIME as shown in Table 5-3E.
- c. Decrease function generator frequency until Counter reads zero. The lowest displayed frequency for a particular measurement time should be within  $\pm 5\%$  of the value shown in Table 5-3E. Record on test card.

Table 5-3E.

MEASUREMENT TIME	LOWEST DISPLAYED FREQUENCY $\pm 5\%$
.01	50 Hz
.04	12.5 Hz
.1	5 Hz
.2	2.5 Hz
.4	1.25 Hz
1	0.5 Hz
2	0.25 Hz
4	0.125 Hz

SENSITIVITY

1. SENSITIVITY MEASUREMENT

- a. Connect Frequency Synthesizer to INPUT using a 50-ohm feedthrough termination. Insert HP 355C and D Variable Attenuators between synthesizer and termination. Connect an RF Voltmeter to the INPUT using a BNC "T" connector.
- b. Set Counter controls as shown in step 2a of frequency tests. Connect the Synthesizer Driver 1 MHz output to Counter time base INPUT connector.
- c. Set synthesizer output frequency to 20 MHz.

Table 5-3. In-Cabinet Performance Check (Cont'd)

SENSITIVITY (Cont'd)

- d. Set attenuators to 0 dB.
- e. Display should be 20.00000 MHz  $\pm$ 1 count. Slowly increase attenuation in 1 dB steps until count becomes unstable. Record the RF voltmeter reading on the test card (should be  $\leq$  100 mVrms).
- f. Disconnect synthesizer from INPUT.

2. PULSE OPERATION

- a. Connect a Pulse Generator to INPUT using a 50-ohm feedthrough termination. Connect oscilloscope in parallel with the input using a BNC "T" connector.
- b. Set Pulse Generator controls for a +300 mV peak-to-peak pulse, 30 nsec wide, at a repetition rate of 10 MHz, measured with oscilloscope.
- c. Set Counter controls as shown in step 2a of frequency tests, except set TIME BASE to INT.
- d. Adjust Counter LEVEL control for a stable displayed count. Display should be 10, MHz. Record value on test card. Repeat 2b through 2d for an amplitude of -300 mV P-P.

3. GATE OUT ANDEXTERNALGATE

- a. Connect Pulse Generator to Counter EXT GATE using 50-ohm feedthrough termination. Connect oscilloscope in parallel with EXT GATE using a BNC "T" connector.
- b. Adjust Pulse Generator for a repetition rate of 10 Hz at maximum pulse width. Adjust the amplitude to +3V P-P.
- c. Remove oscilloscope and "T" connector from EXT GATE.
- d. Connect the oscilloscope to Counter GATE OUT.
- e. Set MODE to CHECK and MEASUREMENT TIME to 4.
- f. Display should be 10 MHz with ARMED and COUNTING lamps alternately flashing (COUNTING lamp may be very dim). Record on test card.
- g. The GATE OUT signal viewed on the oscilloscope should be a 4V P-P (minimum) pulse train at 10 Hz. Record on test card.

4. INTERNAL OSCILLATOR OUTPUT

- a. Connect oscilloscope to the time base INPUT connector.
- b. Verify that the Counter TIME BASE is set to INT.
- c. The internal time base output should be a minimum of 1.0V P-P. Record on test card.

REMOTE PROGRAMMING

1. ENABLE/DISABLE FUNCTIONS

- a. Using a DC Volt-Ohm-Ammeter, with the Counter POWER switch OFF, verify continuity between J6(20) and EXT GATE jack, J6(21) and GATE OUT jack, J6(19) and chassis ground. Record on test card. Refer to Figure 5-2 for J6(REMOTE PROGRAM) connector pin locations.
- b. Set the Counter POWER to ON and measure the dc voltage between J6(1) and chassis ground. The voltage should be +5V  $\pm$ 0.5V. Record on test card.
- c. Connect J6(15) to chassis ground using a clip lead or test box (see Figure 5-2).
- d. By connecting appropriate pins to ground, verify operation of CHECK and HOLD modes, measurement times, RESET, and HYSTERESIS and BLANKING disable. Record on test card.
- e. Remove all external grounds to J6 from steps 1c and 1d and connect oscilloscope between J6(22) and chassis ground. Set MODE to CHECK and MEASUREMENT TIME to .01. PRINT output should be a pulse train with a repetition rate of 100 Hz, pulse width of 15  $\mu$ sec, and amplitude of  $<$  +0.5V with respect to +5V baseline. Record on test card.

Table 5-3. In-Cabinet Performance Check (Cont'd)

POWER SUPPLY REGULATION

1. 115/230 LINE VOLTAGE CHECK

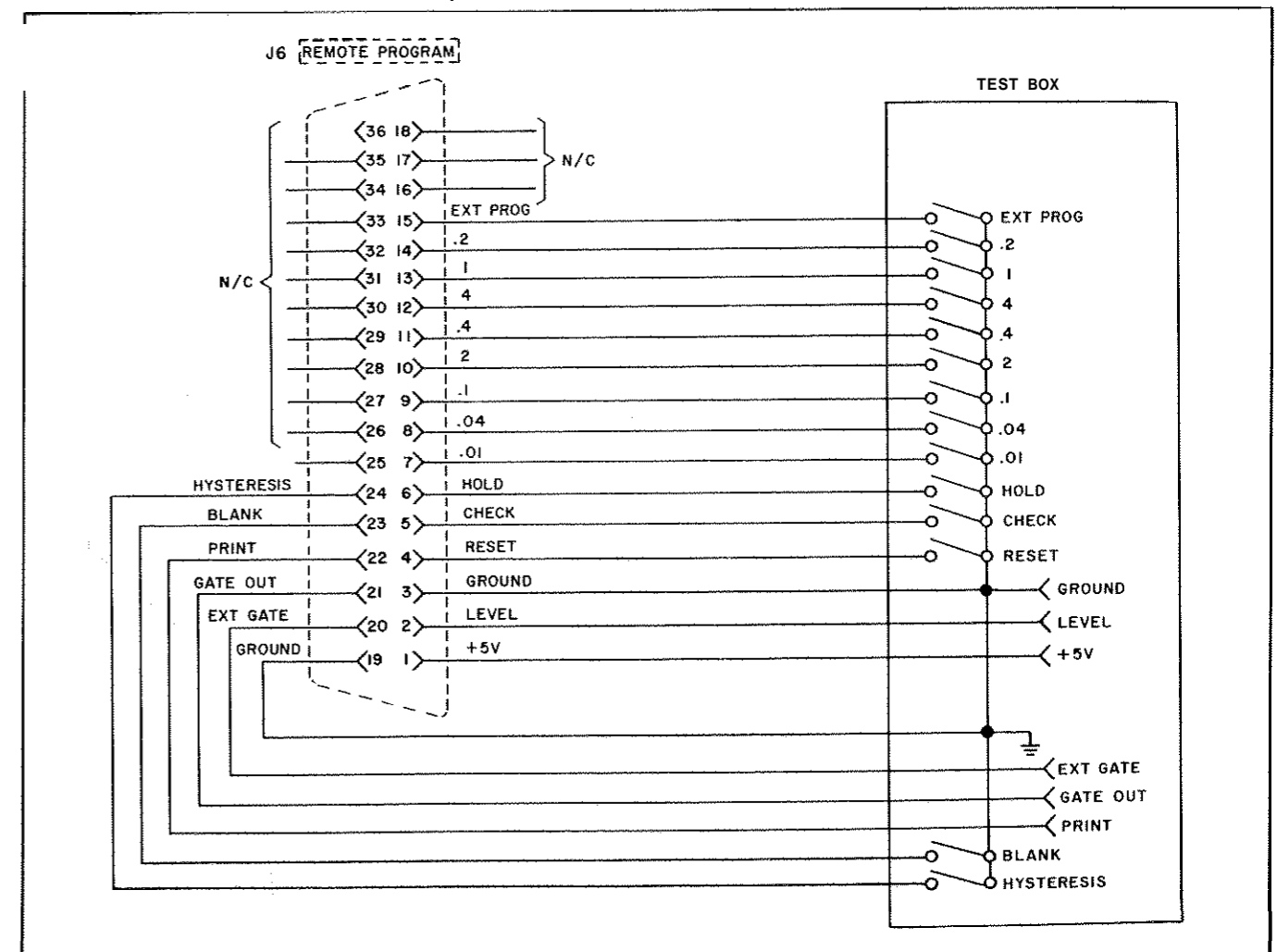
- a. Mark the nominal line voltage used in testing the instrument by making an X in the appropriate box on the test card.
- b. Connect the Counter power cord to a variable ac voltage source. Set ac voltage to LOW LINE (see Table 5-3F). Set Counter POWER to ON.
- c. Connect the DC-Volt-Ohm-Ammeter to J6(1) (+5V). The measured voltage should be +5  $\pm$  0.5 Vdc. Record on test card. Set the Counter POWER to OFF.

Table 5-3F. Line Voltage

Description	115 Volts	230 Volts
LOW LINE	102.0	204.0
NORMAL LINE	115.0	230.0
HIGH LINE	128.0	256.0

- d. Repeat steps 1b and 1c for NORMAL LINE voltage.
- e. Repeat steps 1b and 1c for HIGH LINE voltage.

Figure 5-2. Remote Program Test Box



**PERFORMANCE CHECK TEST CARD**

Hewlett-Packard Model 5323A Automatic Counter Serial No. _____	Tests Performed by _____ Date _____
Description	Check
<b>FREQUENCY/RPM MEASUREMENTS</b>	
1. SELF-CHECK	_____ 10.00000 MHz
2. DECIMAL POINT/MEASUREMENT UNITS	
Display _____ NN. NNNNN MHz (N = any digit, but not blanked) _____ N. NNNNNN MHz (X = blank digit) _____ NNN. NNNN kHz _____ NN. NNNNN kHz _____ N. NNNNNN kHz _____ NNN. NNNN Hz _____ NN. NNNNN Hz _____ 0. XXXXXX Hz	
Printed Exponent	_____ 7 _____ 6 _____ 5 _____ 4 _____ 3 _____ 2 _____ 1 _____ 0
3. ACCURACY	
Display/Printed Value	_____ 1. 11111 MHz ±1 Count _____ 2. 22222 MHz ±1 Count _____ 3. 33333 MHz ±1 Count _____ 4. 44444 MHz ±1 Count _____ 5. 55555 MHz ±1 Count _____ 6. 66666 MHz ±1 Count _____ 7. 77777 MHz ±1 Count _____ 8. 88888 MHz ±1 Count _____ 9. 99999 MHz ±1 Count
4. HYSTERESIS	
Enabled	_____ ,98888 MHz
Disabled	_____ 988.8888 kHz

PERFORMANCE CHECK TEST CARD

Description		Check
<b>FREQUENCY/RPM MEASUREMENTS</b>		
<b>5. BLANKING</b>		
Enabled		2 MHz
	4	7 digits
	2	7 digits
	1	7 digits
	.4	7 digits
	.2	6 digits
	.1	6 digits
	.04	5 digits
	.01	5 digits
Enabled		1 MHz
	4	7 digits
	2	7 digits
	1	7 digits
	.4	7 digits
	.2	7 digits
	.1	7 digits
	.04	6 digits
	.01	6 digits
Enabled (with Hysteresis)		9.888888 MHz
	4	6 digits
	2	6 digits
	1	6 digits
	.4	6 digits
	.2	6 digits
	.1	6 digits
	.04	5 digits
	.01	5 digits
Disabled		.01
		7 digits
<b>6. RPM</b>		
Display		600.00N RPM
(N = any digit, but not blanked)		60.000N RPM
		6.0000N RPM
		60000N. RPM
		60000. N RPM
		6000. NN RPM
		0. RPM

PERFORMANCE CHECK TEST CARD

Description		Check
<b>FREQUENCY/RPM MEASUREMENTS (Cont'd)</b>		
<b>6. RPM (Cont'd)</b>		
Low Frequency	10 Hz	600.000 RPM $\pm 2\%$
	1 Hz	60.0000 RPM $\pm 2\%$
	0.1 Hz	6.00000 RPM $\pm 2\%$
<b>RESET AND HOLD</b>		
<b>1. RESET</b>		
		Reset to zero
		1 kHz $\pm 2\%$
		Reset to zero
		ARMED lamp ON
		COUNTING lamp ON
		1 kHz $\pm 2\%$
<b>2. HOLD</b>		
		1.1 kHz $\pm 2\%$
		Reset to zero
		1.1 kHz $\pm 2\%$
<b>3. LOW-FREQUENCY RESET</b>		
	.01	50 Hz $\pm 5\%$
	.04	12.5 Hz $\pm 5\%$
	.1	5 Hz $\pm 5\%$
	.2	2.5 Hz $\pm 5\%$
	.4	1.25 Hz $\pm 5\%$
	1	0.5 Hz $\pm 5\%$
	2	0.25 Hz 15%
	4	0.125 Hz $\pm 5\%$
<b>SENSITIVITY</b>		
<b>1. SENSITIVITY MEASUREMENT</b>		
		20.00000 MHz $\pm 1$ Count
		100 mVrms, maximum
<b>2. PULSE OPERATION</b>		
	+ Pulse	10 MHz
	- Pulse	10 MHz
<b>3. GATE OUT AND EXTERNAL GATE</b>		
		10.00000 MHz
		4V P-P, minimum
<b>4. INTERNAL OSCILLATOR OUTPUT</b>		
		1.0V P-P, minimum



PERFORMANCE CHECK TEST CARD

Table 5-4. Adjustments

Description		Check
<b>REMOTE PROGRAMMING</b>		
1. ENABLE/DISABLE FUNCTIONS	J6(20) _____	continuity to EXT GATE
	J6(21) _____	continuity to GATE OUT
	J6(3) _____	continuity to chassis
	J6(19) _____	continuity to chassis
	J6(1) _____	+5 ± 0.5 Vdc
	Check _____	verified
	Hold _____	verified
	.01 _____	verified
	.04 _____	verified
	.1 _____	verified
	.2 _____	verified
	.4 _____	verified
	1 _____	verified
	2 _____	verified
	4 _____	verified
	Reset _____	verified
	Hysteresis _____	verified
	Blanking _____	verified
	Print _____	100 Hz
		15 μsec
		+0.5 Vdc, maximum
<b>POWER SUPPLY REGULATION</b>		
115/230 LINE VOLTAGE CHECK AT J6(1)	115V <input type="checkbox"/>	230V <input type="checkbox"/>
	LOW _____	+5 ± 0.5 Vdc
	NORM _____	+5 ± 0.5 Vdc
	HIGH _____	+5 ± 0.5 Vdc

NOTE: All voltage measurements with respect to chassis

1. INPUT AMPLIFIER A2

The following procedure sets the sensitivity of the input amplifier and checks the frequency response.

a. Set Counter controls as follows:

MODE . . . . .	NORM
MEASUREMENT TIME . . . . .	.4
LEVEL . . . . .	PRESET
ATTEN. . . . .	X1
AC-DC . . . . .	DC
Hz/RPM . . . . .	Hz
BLANKING . . . . .	ON
HYSTERESIS . . . . .	ON
TIME BASE . . . . .	INT

- b. Connect HP 3200B to HP 355C and 355D attenuators connected in series. Set attenuators to zero dB and connect through 50-ohm feedthrough termination to Counter INPUT.
- c. Set HP 32000 controls for 20 MHz output as indicated by Counter Display.
- d. Increase attenuator settings until Counter Display becomes erratic or reads zero.
- e. Adjust A2R10 for a stable 20 MHz display.
- f. Repeat steps d and e until A2 Amplifier is peaked.
- g. Measure Counter input using HP 411A RE' voltmeter. Minimum input level for stable display should be 100 mV.

2. OSCILLATOR/MULTIPLIER ASSEMBLY A14

- a. Set Counter TIME BASE switch to EXT.
- b. Connect a 1 MHz standard frequency to time base INPUT connector.
- c. Connect oscilloscope through a 10:1 probe to A14(1).

Note

Do not use extender board during adjustments

- d. Adjust oscilloscope controls for a stable display.
- e. Adjust L2, L3, L4, and L5 for maximum output on oscilloscope (should be greater than 2V P-P). Disconnect all test equipment.
- f. Set Counter TIME BASE switch to INT.
- g. Connect an HP 5245M Electronic Counter to time base INPUT connector.
- h. Adjust A14C5 for 10 MHz ± 11 Hz.

Note

If crystal or heater (A15 Assy) has been changed, it may be necessary to select C4 to permit tuning to 10 MHz.

- i. Clip current probe over the orange wire from A14(12). Connect the probe through probe amplifier to oscilloscope input. Set oscilloscope to .05V/cm and probe amplifier to 5mA/cm.
- j. Adjust A14R6 for 20 mA P-P on oscilloscope.
- k. Readjust A14C5 for 10 MHz ± 1 count on electronic counter.

3. POWER SUPPLY ADJUSTMENTS

No power supply adjustments are necessary. If power supplies fail, remove ac power and press A17S1 RESET switch. Return Counter ac power on. If supplies are still off or low, determine cause by troubleshooting.

5-27. TROUBLESHOOTING

5-28. Troubleshooting Aids

5-29. THEORY OF OPERATION. Section IV provides information with a flow chart on Counter operation in all modes.

5-30. SCHEMATIC DIAGRAMS. Schematic diagrams, waveforms, and operation and troubleshooting of individual assemblies are provided in Section VIII.

5-31. COMPONENT LOCATION. Photographs of printed circuit assemblies with component callouts are included in Section VIII with the schematics.

5-32. TROUBLESHOOTING PROCEDURE

5-33. The following paragraphs, steps, and charts aid in locating problems. Use this section to isolate trouble to an assembly; then go to that assembly schematic and operation in Section VIII to locate the defective components. The Flow Diagram and Block Diagram should be referred to during the following discussion; these may be folded out from Section VIII.

5-34. TROUBLE AT TURN ON. If Counter fails to turn on (no display, decimal point, measurement unit, or COUNTING/ARM display) make the following checks:

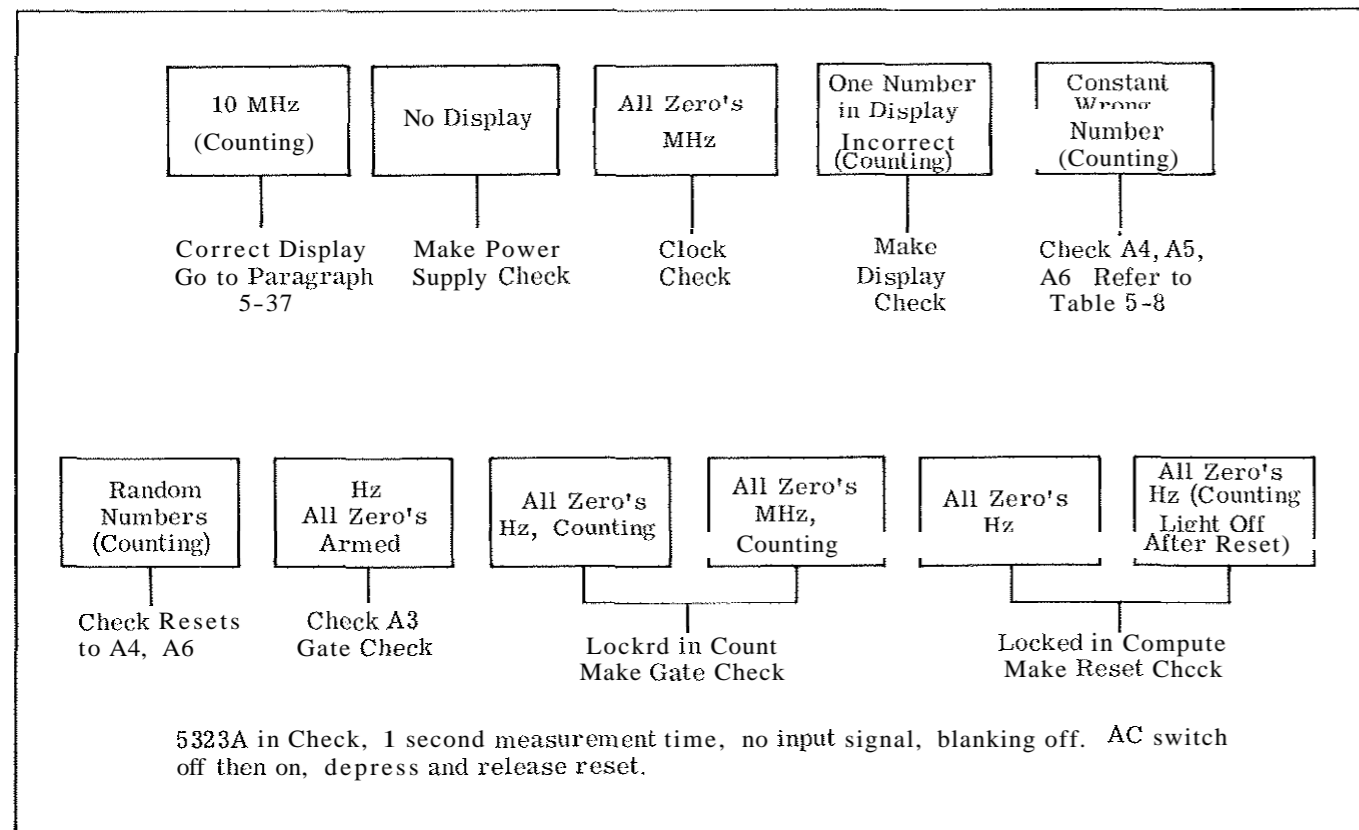
- a. Line voltage switch set for correct voltage (115V or 230V).
- b. Power cord plugged into counter and power source.
- c. Line fuse good.
- d. AC power available at source.
- e. Check A16, A17, T1, L1, and L2

Note

The +5.1V output from A16 is available at J7. The +12V output from A17 is available at a test point located between J7 and A15.

5-35. TROUBLE DURING SELF CHECK. Refer to Table 5-5, the diagnostic tree for the Counter. Five troubleshooting routines are indicated: power supply, clock, reset, gate and display check. The power supply check has been discussed in paragraph 5-34. When using an oscilloscope to troubleshoot, a fast MEASUREMENT TIME setting is useful. The .01 setting may be used, or a HNC cable may be connected from GATE OUT to EXT GATE on the rear panel of the Counter (use a BNC Tee to provide external trigger for the oscilloscope).

Table 5-5. 5323A Diagnostic Tree



5-36. CLOCK CHECK

a. Check the 10 MHz internal time base signal at time base INPUT with TIME BASE set to INT. The signal should be 10 MHz, 1.0V P-P (minimum) into a 50-ohm load. If signal frequency or amplitude are incorrect, go to A14, A15.

b. Check for clock input (Fy) at pin C of A3. Go to A9 and interconnecting coaxial cable if signal is absent.

c. Check for CLOCK output at pin N of A3. If no signal, make sure that MODE is not in HOLD. If frequency is not Fy, but Fy/6, check Hz/RPM switch, then go to A3.

d. Check for CLOCK input at pin C of A7. Go to A9 if signal is absent.

5-37. RESET CHECK

a. Hold RESET depressed or connect a clip-lead from the BRN wire of the RESET switch to chassis ground.

Note

The ARMED light will go dim in this state. Use a Logic Probe to verify the following conditions.

b. Check A3: should be HIGH on pins 12 and 13, LOW on pin K.

c. Check A4: Xa, Xb, Xc, Xd should be LOW.

d. Check A5: Σa, Cb, Zc, Σd should be HIGH.

e. Check A6: Ya, Yb, Yc, Yd should be LOW.

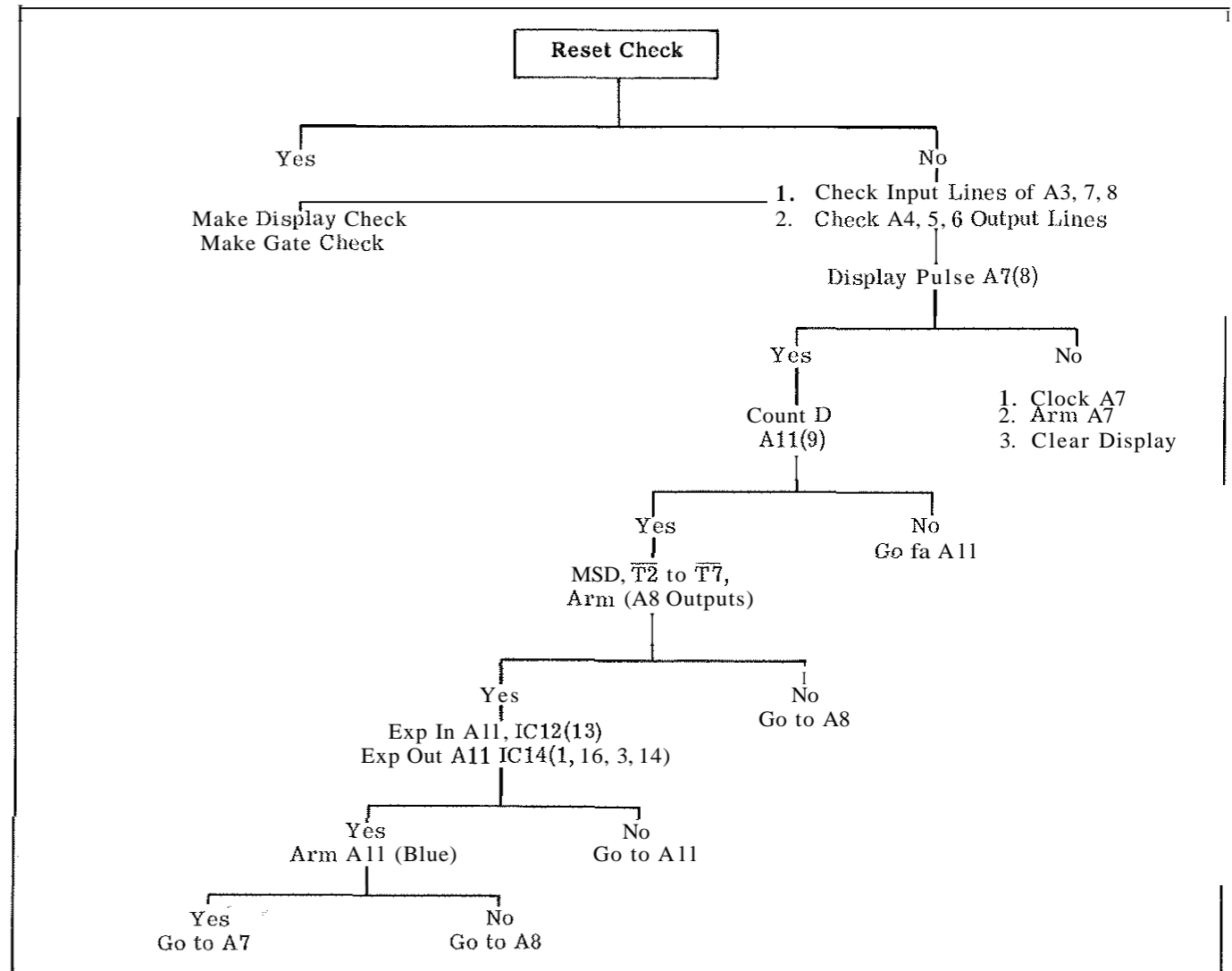
f. Check A7: should be HIGH on pins 10 and 14.

g. Check A8: should be HIGH on pin 5.

h. If the above tests with the Logic Probe indicate a malfunction, refer to Table 5-6 for a more detailed procedure.

i. Remove the clip-lead from the RESET switch after troubleshooting.

Table 5-6. Reset Check Tree



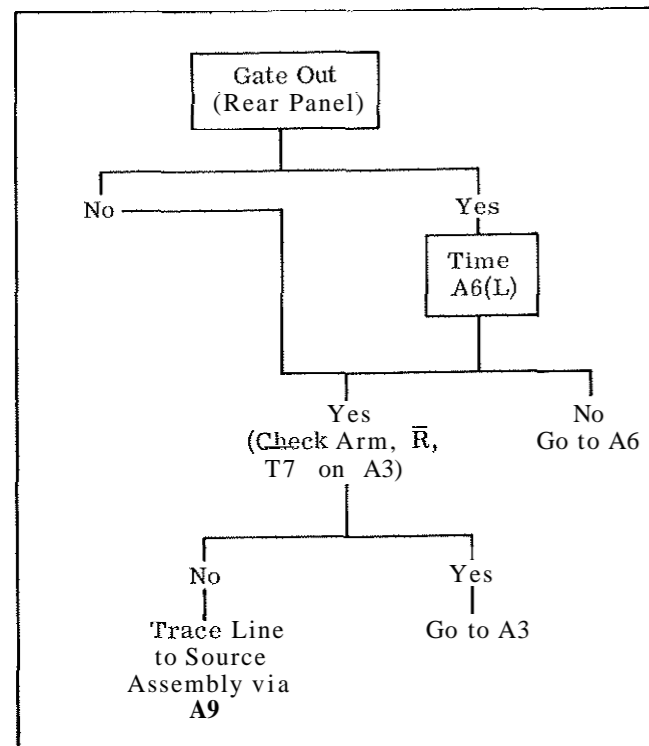
5-38. GATE CHECK

- a. Set MODE to CHECK, MEASUREMENT TIME to 1, Hz/RPM to Hz, and TIME BASE to INT.
- b. Check A3: should be HIGH on pins 3, 10, L, and P, LOW on pin E.
- c. Refer to Table 5-7 for more detailed troubleshooting procedure.

5-39. DISPLAY CHECK

- a. With MODE set to CHECK and MEASUREMENT TIME set to 1, connect a clip-lead from A11IC8(4) (test point is provided between IC15 and IC19) to chassis ground. Display should step from all ones to all twos, etc., to all nines. Last digit (LSD) of the all nines display will be a zero which is normal. The all zero display will be skipped which is also normal. If all numbers appear and the display steps from ones to nines, the display is normal. Remove the clip-lead.
- b. If the display steps correctly, but a wrong number appears such as a three when all eights are displayed, set MODE to HOLD to freeze the incorrect display. Trc BCD lines from the A11 and A12 boards can now be checked with the Logic Probe.
- c. A digit that will not change may be caused by a missing transfer pulse (MSD, T2 through T7). Go to A8.
- d. If the display does not step, make Reset Check (paragraph 5-34). If reset is correct, go to A7.

Table 5-7. Gate Check Tree



e. A blanked display tube can be caused by a defective display tube or blank input. Go to A12.

f. If a constant wrong number is displayed with the Counter MODE set to CHECK (A11 test point not grounded), the problem should be in A4, A5, or A6. Check the X, Y, I and Σ lines, because a line is probably held HIGH or LOW. Refer to Table 5-8 which lists typical defective displays and their causes.

5-40. ADDITIONAL TESTS

- a. If the Counter correctly displays 10.00000 MHz, check to verify that it resets.
- b. Make a display check to see if all numbers appear.
- c. Check all MEASUREMENT TIME settings. Reset at each setting. If trouble occurs, go to A10.
- d. With MODE set to NORM, verify that ARM light is ON with no input signal. If trouble occurs, go to A13.
- e. Connect a signal to INPUT and verify operation to 20 MHz and to 100 mV sensitivity. This will check the A1 and A2 assemblies.
- f. Check operation of the Hz/RPM switch in RPM. Fy should be divided by 6 in A3 and appear at pin N. All measurement times are now multiplied by 6.

g. Check blanking, hysteresis, and external gate operation.

Table 5-8. Defective Displays

Display (COUNTING and MHz ON)	Check Line for Signal:
10.11111	Ib, Id
11.11111	Xd, C2
11.22222	Σd
12.11118	Ia
12.22222	Xc
15.55555	Σa
2.111111	Ic
21.11111	Ic
24.44444	Σb
25.55555	Xa
42.22222	Xc, Ic, Σc
44.44444	Xb
99.99999	C2

SECTION VI  
REPLACEABLE PARTS

6-1. INTRODUCTION

6-2. This section contains information for ordering replacement parts. Table 6-1 lists parts in alpha-numerical order of their reference designators and indicates the description and HP part number of each part, together with any applicable notes. Table 6-2 lists parts in alpha-numerical order of their HP part number and provides the following information on each part:

- a. Description of part (see abbreviations below).
- b. Typical manufacturer of the part in a five-digit code; see list of manufacturers in Table 6-3.
- c. Manufacturer's part number.
- d. Total quantity used in the instrument (TQ column).

6-3. Miscellaneous parts are listed at the end of Table 6-1.

6-4. ORDERING INFORMATION

6-5. To obtain replacement parts, address order or inquiry to your local Hewlett-Packard Sales and Service office (see lists at rear of this manual for addresses). Identify parts by their Hewlett-Packard part numbers.

6-6. To obtain a part that is not listed, include:

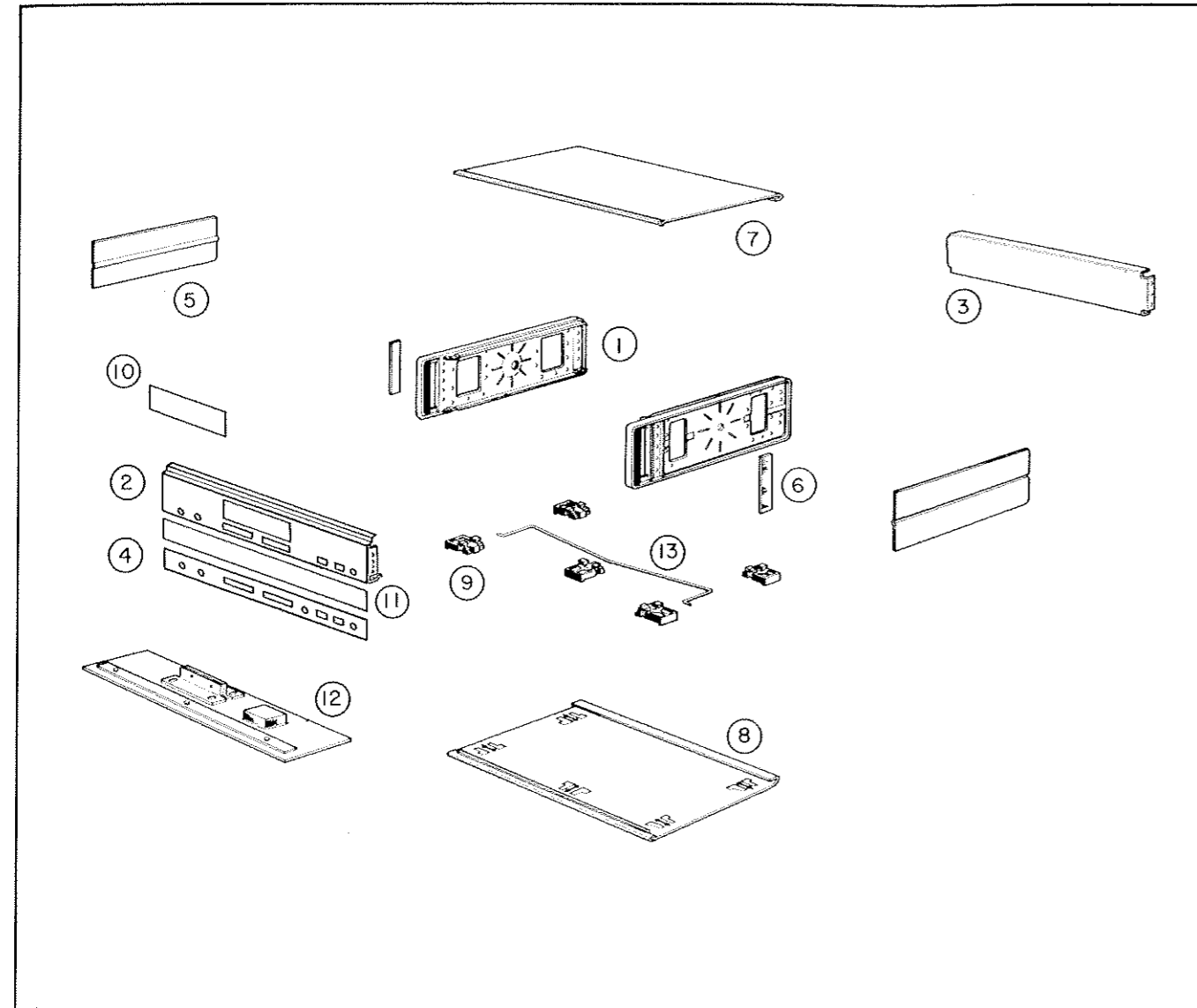
- a. Instrument model number.
- b. Instrument serial number.
- c. Description of the part.
- d. Function and location of the part.

REFERENCE DESIGNATORS			
A = assembly	F = fuse	MP = mechanical part	U = integrated circuit
B = motor	FL = filter	P = plug	V = vacuum tube, neon bulb, photocell, etc.
BT = battery	IC = integrated circuit	Q = transistor	VR = voltage regulator
C = capacitor	J = jack	R = resistor	W = cable
CP = coupler	K = relay	RT = thermistor	X = socket
CR = diode	L = inductor	S = switch	Y = crystal
DL = delay line	LS = loud speaker	T = transformer	Z = tuned cavity, network
DS = device signaling (lamp)	M = meter	TB = terminal board	
E = miscellaneous electronic part	MK = microphone	TP = test point	

ABBREVIATIONS			
A = amperes	H = henries	N/O = normally open	RMO = rack mount only
AFC = automatic frequency control	HDW = hardware	NOM = nominal	RMS = root-mean square
AMPL = amplifier	HEX = hexagonal	NPO = negative positive zero (zero temperature coefficient)	RWV = reverse working voltage
BFO = beat frequency oscillator	HR = hour(s)	NPN = negative-positive-negative	S-B = slow-blow
BE CU = beryllium copper	HZ = hertz	NRFR = not recommended for field replacement	SCR = screw
BH = binder head	IF = intermediate freq	NSR = not separately replaceable	SE = selenium
BP = bandpass	IMPG = impregnated		SECT = section(s)
BRS = brass	INCND = incandescent		SEMICON = semiconductor
BWO = backward wave oscillator	INCL = include(s)		SI = silicon
CCW = counter-clockwise	INS = insulation (cd)		SIL = silver
CER = ceramic	INT = internal	OBD = order by description	SL = slide
CMO = cabinet mount only	K = kilo = 1000	OH = oval head	SPG = spring
COEF = coefficient	LH = left hand	OX = oxide	SPI = special
COM = common	LEN = linear taper	P = peak	SST = stainless steel
COMP = composition	LK WASH = lock washer	PC = printed circuit	SR = split ring
COMPL = complete	LOG = logarithmic taper	PF = picofarads = 10 <sup>-12</sup>	STL = steel
CONN = connector	LPF = low pass filter	PH BRZ = phosphor bronze	TA = tantalum
CP = cadmium plate	M = milli = 10 <sup>-3</sup>	PHL = Phillips	TD = time delay
CRT = cathode-ray tube	MEG = meg = 10 <sup>6</sup>	PIV = peak inverse voltage	TGL = toggle
CW = clockwise	MET FLM = metal film	PNP = positive-negative-positive	THD = thread
DEPC = deposited carbon	MET OX = metallic oxide	P/O = part of	TI = titanium
DR = drive	MFR = manufacturer	POLY = polystyrene	TOL = tolerance
ELECT = electrolytic	MHZ = mega hertz	PORC = porcelain	TRIM = trimmer
ENCAP = encapsulated	MINAT = miniature	POS = position(s)	TWT = traveling wave tube
EXT = external	MOM = momentary	POT = potentiometer	U = micro = 10 <sup>-6</sup>
F = farads	MOS = metal oxide substrate	PP = peak-to-peak	VAR = variable
FH = flat head	MTG = mounting	PT = point	VDCW = dc working volts
FIL H = fillister head	MY = "mylar"	PWV = peak working voltage	W = with
FXD = fixed	N = nano (10 <sup>-9</sup> )	RECT = rectifier	W = watts
G = giga (10 <sup>9</sup> )	N/C = normally closed	RF = radio frequency	WIV = working inverse voltage
GE = germanium	NE = neon	RH = round head or right hand	WV = wirewound
GL = glass	NI PL = nickel plate		W/O = without
GRD = ground(ed)			

Figure 6-1. Modular Cabinet Parts



Item No.	Description	HP Part Number
1	Side Frame Assembly	5060-0729
2	Front Panel	05323-00001
3	Rear Panel	05323-00004
4	Bottom Extrusion Panel	05323-00003
5	Side Frame Cover	5000-0729
6	Side Trim	5000-0050
7	Top Cover	05325-00008
8	Bottom Cover Assembly	05325-60032
9	Foot Assembly	5060-40001
10	Light Mask	05323-40002
11	Light Bezel Mask	05323-80001
12	Rack Mount Kit	05325-60031
13	Tilt Stand	1490-0030

Table 6-1. Reference Designation Index

Reference Designation	Part No.	Description #	Note
A2CR2	1901-0376	DIODE:SILICON 35V	
A2CR3	1901-0376	DIODE:SILICON 35V	
A2CR4	1901-0040	DIODE:SILICON 30MA 30MV	
A2CR5	1901-0040	DIODE:SILICON 30MA 30MV	
A2CR6	1901-0040	DIODE:SILICON 30MA 30MV	
A2CR7	1910-0032	DIODE:GERMANIUM 5 MIV	
A2CR8	1910-0032	DIODE:GERMANIUM 5 MIV	
A2CR9	1910-0032	DIODE:GERMANIUM 5 MIV	
A2CR10	1901-0460	DIODE:SILICON 3 JUNCTION STABILISOR	
A2CR11	1901-0040	DIODE:SILICON 30MA 30MV	
A2CR12	1901-0040	DIODE:SILICON 30MA 30MV	
A2Q1	1855-0320	TRANSISTOR:DUAL PNP SILICON	
A2Q2	1853-0015	TRANSISTOR:SILICON PNP 2N3640	
A2Q3	1854-0071	TRANSISTOR:SILICON PNP	
A2Q4	1853-0015	TRANSISTOR:SILICON PNP 2N3640	
A2Q5	1854-0019	TRANSISTOR:SILICON PNP	
A2Q6	1854-0071	TRANSISTOR:SILICON PNP	
A2Q7	1854-0019	TRANSISTOR:SILICON PNP	
A2Q8	1854-0009	TRANSISTOR:SILICON PNP 2N709	
A2Q9	1854-0009	TRANSISTOR:SILICON PNP 2N709	
A2Q10	1853-0036	TRANSISTOR:SILICON PNP	
A2Q11	1854-0009	TRANSISTOR:SILICON PNP 2N709	
A2R1	0683-5125	R:FXD COMP 5100 OHM 5% 1/4W	
A2R2	0683-5125	R:FXD COMP 5100 OHM 5% 1/4W	
A2R3	0683-1045	R:FXD COMP 100K OHMS 5% 1/4W	
A2R4	0683-1045	R:FXD COMP 10K OHM 5% 1/4W	
A2R5	0683-6815	R:FXD COMP 680 OHM 5% 1/4W	
A2R6	0683-4725	R:FXD COMP 4700 OHM 5% 1/4W	
A2R7	0683-1205	R:FXD COMP 1200 OHM 5% 1/4W	
A2R8	0683-4315	R:FXD COMP 430 OHM 5% 1/4W	
A2R9	0683-3105	R:FXD COMP 91 OHM 5% 1/4W	
A2R10	2100-1757	R:VAR WH 500 OHM 10% LIN 1/2W	
A2R11	0683-2015	R:FXD COMP 200 OHM 5% 1/4W	
A2R12	0683-9105	R:FXD COMP 91 OHM 5% 1/4W	
A2R13	0683-1045	R:FXD COMP 100K OHMS 5% 1/4W	
A2R14	0683-1045	R:FXD COMP 10K OHM 5% 1/4W	
A2R15	0683-5105	R:FXD COMP 51 OHM 5% 1/4W	
A2R16	0683-6815	R:FXD COMP 680 OHM 5% 1/4W	
A2R17	0683-3315	R:FXD COMP 330 OHM 5% 1/4W	
A2R18	0683-3315	R:FXD COMP 330 OHM 5% 1/4W	
A2R19	NOT ASSIGNED		
A2R20	NOT ASSIGNED		
A2R21	0683-2715	R:FXD COMP 270 OHM 5% 1/4W	
A2R22	0683-1045	R:FXD COMP 100K OHM 5% 1/4W	
A2R23	0683-2705	R:FXD COMP 2700 OHM 5% 1/4W	
A2R24	0683-1535	R:FXD COMP 15K OHM 5% 1/4W	
A2R25	0683-1235	R:FXD COMP 12K OHM 5% 1/4W	

# See introduction to this section for ordering information

Reference Designation	Part No.	Description #	Note
A1	05E23-000 6	BOARD ASSY:ATTENUATOR	
A1C1	05E23-2000 6	BOARD:BLANK PC	
A1C2	0 10-0180	C:FXD MY 0.033 UF 50	
A1C3	0 14-0229	C:FXD MICA 5.0 PF 10% 50V	
A1C4	0 14-0201	C:FXD MICA 51 PF 5% 50V	
A1J1	0 14-034	C:FXD MICA 500 PF 1%	
A1R1	1 25-113	CONNECTOR:RNC INPUT	
A1R2	0 68-1045	R:FXD COMP 100K OHMS 5% 1/4W	
A1R3	0 68-1045	R:FXD COMP 10K OHM 5% 1/4W	
A1	5 04-025	SWITCH:LEVER	
	5 02-130	SPRING:DETENT	
	5 04-021	SLIDE:POLE	
	5 02-242	SPRING:CONTACT	
	0 53-210 15	GUIDE:SWITCH	
A2	0 53-6035	BOARD ASSY:AMPLIFIER	
A2C1	0 5E25-200 35	BOARD:BLANK PC	
A2C2	0 18-010	C:FXD ELECT 3.3 UF 20% 15VDCW	
A2C3	0 18-010	C:FXD ELECT 3.3 UF 20% 15VDCW	
A2C6	0 18-173	NOT ASSIGNED	
A2C7	0 14-032	C:FXD ELECT 0.1 UF 10% 35VDCW	
A2C8	0 14-032	C:FXD MICA 68 PF 5%	
A2C9	0 16-255	C:FXD CER 8.2 0.25 PF 500VDCW	
A2C10	0 18-010	C:FXD ELECT 3.3 UF 20% 15VDCW	
A2C11	0 16-255	C:FXD CER 8.2 0.25 PF 500VDCW	
A2C12	0 18-020	C:FXD ELECT 3.3 UF 20% 15VDCW	
A2C13	0 16-016	C:FXD MICA 24PF 5% 300VDCW	
A2C14	0 16-016	C:FXD MICA 24PF 5% 300VDCW	
A2C15	0 18-020	C:FXD ELECT 3.3 UF 20% 15VDCW	
A2C16	0 16-228	C:FXD CER 4.3 0.25 PF 500VDCW	
A2C17	0 16-033	C:FXD CER 0.01 UF 80-28% 100VDCW	
A2C18	0 16-033	C:FXD MICA 15 PF 0.5 PF	
A2C19	0 16-221	C:FXD CER 2.2-0.25 PF 500VDCW	
A2C20	0 15-000	C:FXD CER 1000 PF 600VDCW	
A2C21	0 16-219	C:FXD MICA 30 PF 5%	
A2CR1	1 90-040	DIODE:SILICON 30MA 30MV	

# See introduction to this section for ordering information













Table 6-3. Code List of Manufacturers (Cont'd)

Code No.	Manufacturer	Address	Code No.	Manufacturer	Address	Code No.	Manufacturer	Address
80486	All Star Products Inc.	Defiance, Ohio	86684	Radio Corp. of America, Electronic		95566	Arnold Engineering Co.	Marengo, Ill.
80509	Avery Label Co.	Monrovia, Calif.		Comp. & Devices Div.	Harrison, N. J.	95712	Dage Electric Co., Inc.	Franklin, Ind.
80583	Hammahnd Co., Inc.	Mars Hill, N. C.	86928	Seastrom Mfg. Co.	Glendale, Calif.	95984	Siemon Mfg. Co.	Wayne, Ill.
80640	Stevens, Arnold, Co., Inc.	Boston, Mass.	87034	Marco Industries	Anaheim, Calif.	95987	Weckesser Co.	Chicago, Ill.
80813	Dinco Gray Co.	Dayton, Ohio	87216	Philco Corporation (Lansdale Division)	Lansdale, Pa.	96067	Microwave Assoc., West Inc.	Sunnyvale, Calif.
81030	International Instruments Inc.	Orange, Conn.	87473	Westein Fibrous Glass Products Co.	San Francisco, Calif.	96095	Hi-Q Div. of Aerovox Corp.	Olean, N. Y.
81073	Grayhill Co.	LaGrange, Ill.				96256	Thordarson-Meissner Inc.	ML Carmel, Ill.
81095	Triad Transformer Corp.	Venice, Calif.	87664	Van Waters & Rogers Inc.	San Francisco, Calif.	96296	Solar Manufacturing Co.	Los Angeles, Calif.
81312	Winchester Elec. Div. Litton Ind., Inc.	Dakville, Conn.	87930	Tower Mfg. Corp.	Providence, R. I.	96306	Microswitch, Div. of Minn.-Honeywell	Freeport, Ill.
81349	Military Specification		88140	Cutter-Hammer, Inc.	Lincoln, Ill.	96330	Carlton Screw Co.	Chicago, Ill.
81483	International Rectifier Corp.	El Segundo, Calif.	88220	Gould-National Batteries, Inc.	St. Paul, Minn.	96341	Microwave Associates, Inc.	Burlington, Mass.
81541	Anipax Electronics, Inc.	Cambridge, Maryland	88598	General Mills, Inc.	Buffalo, N. Y.	96501	Excel Transformer Co.	Oakland, Calif.
81860	Barry Controls, Div. Barry Wright Corp.	Watertown, Mass.	89231	Graybar Electric Co.	Oakland, Calif.	96508	Xcelite Inc.	Orchard Park, N. Y.
82042	Carter Precision Electric Co.	Skokie, Ill.	89473	G. E. Distributing Corp.	Schenectady, N. Y.	96733	San Fernando Elect. Mfg. Co.	San Fernando, Calif.
82047	Sperit Faraday Inc., Copper Hewitt Electric Div.	Hoboken, N. J.	89665	United Transformer Co.	Chicago, Ill.	96881	Thomson Ind. Inc.	Long Is., N. Y.
82116	Electric Regulator Corp.	Norwalk, Conn.	90030	United Shoe Machinery Corp.	Beverly, Mass.	97464	Industrial Retaining Ring Co.	Irrington, N. J.
82142	Jellefs Electronics Division of Speer Carbon Co.	Du Bois, Pa.	90179	US Rubber Co., Consumer Ind. & Plastics Prod. Div.	Passaic, N. J.	97539	Automatic & Precision Mfg.	Englewood, N. J.
82170	Fairchild Camera & Inst. Corp. Space & Defense System Div.	Paramus, N. J.	90763	United Carr Fastener Corp.	Chicago, Ill.	97929	Reon Resistor Corp.	Yonkers, N. Y.
82209	Maguire Industries, Inc.	Greenwich, Conn.	90970	Bearing Engineering Co.	San Francisco, Calif.	97983	Lifton System Inc., Adler-Westrex Comm. Div.	New Rochelle, N. Y.
82219	Sylvania Electric Prod. Inc. Electronic Tube Division	Emporium, Pa.	91146	ITT Cannon Elect. Inc., Salem Div.	Salem, Mass.	98141	R-Tronics, Inc.	Jamaica, N. Y.
82376	Astron Corp.	East Newark, Harrison, N. J.	91260	Connor Spring Mfg. Co.	San Francisco, Calif.	98159	Rubber Teck, Inc.	Gardena, Calif.
82389	Switchcraft, Inc.	Chicago, Ill.	91345	Miller Dial & Nameplate Co.	El Monte, Calif.	98220	Hewlett-Packard Co., Moseley Div.	Pasadena, Calif.
82647	Metals & Controls Inc. Spencer Products	Attleboro, Mass.	91418	Radio Materials Co.	Chicago, Ill.	98278	Microdol, Inc.	So. Pasadena, Calif.
82768	Phillips-Advance Control Co.	Joliet, Ill.	91506	Augal Inc.	Attleboro, Mass.	98291	Sealectro Corp.	Mamaroneck, N. Y.
82866	Research Products Corp.	Madison, Wis.	91637	Dale Electronics, Inc.	Columbus, Nebr.	98376	Zero Mfg. Co.	Burbank, Calif.
82877	Rotron Mfg. Co., Inc.	Woodstock, N. Y.	91662	Elco Corp.	Willow Grove, Pa.	98410	Etc Inc.	Cleveland, Ohio
82893	Vector Electronic Co.	Glendale, Calif.	91737	Grenar Mfg. Co., Inc.	Wakefield, Mass.	98731	General Mills Inc., Electronics Div.	Minneapolis, Minn.
83014	Hartwell Corp.	Los Angeles, Calif.	91827	K F Development Co.	Redwood City, Calif.	98734	Paeco Div. of Hewlett-Packard Co.	Palo Alto, Calif.
83058	Carr Fastener Co.	Cambridge, Mass.	91886	Malco Mfg. Co., Inc.	Chicago, Ill.	98821	North Hills Electronics, Inc.	Glen Cove, N. Y.
83086	New Hampshire Ball Bearing, Inc.	Peterborough, N. H.	91929	Honeywell Inc., Micro Switch Div.	Freeport, Ill.	98978	International Electronic Research Corp.	Burbank, Calif.
83125	General Instrument Corp., Capacitor Div.	Darlington, S. C.	91961	Nahn-Bros. Spring Co.	Oakland, Calif.	99109	Columbia Technical Corp.	New York, N. Y.
83148	ITT Wire and Cable Div.	Los Angeles, Calif.	92180	Tru-Connector Corp.	Peabody, Mass.	99313	Varian Associates	Palo Alto, Calif.
83186	Victory Eng. Corp.	Springfield, N. J.	92367	Eigeel Optical Co. Inc.	Rochester, N. Y.	99378	Atlee Corp.	Winchester, Mass.
83298	Bendix Corp., Red Bank Div.	Red Bank, N. J.	92607	Tensolite Insulated Wire Co., Inc.	Tarrytown, N. Y.	99515	Marshall Ind., Capacitor Div.	Monrovia, Calif.
83315	Hubbell Corp.	Mundelein, Ill.	92702	IMC Magnetics Corp.	Westbury Long Island, N. Y.	99707	Control Switch Division, Controls Co. of America	El Segundo, Calif.
83324	Rosan Inc.	Newport Beach, Calif.	92966	Hudson Lamp Co.	Keaneey, N. J.	99800	Delevan Electronics Corp.	East Aurora, N. Y.
83330	Smith, Herman H., Inc.	Brooklyn, N. Y.	93332	Sylvania Electric Prod. Inc. Semiconductor Div.	Woburn, Mass.	99848	Wilco Corporation	Indianapolis, Ind.
83332	Tech Labs	Palisades Park, N. J.	93369	Robbins & Myers Inc.	Palisades Park, N. J.	99928	Branson Corp.	Whippany, N. J.
83385	Central Screw Co.	Chicago, Ill.	93410	Slemco Controls, Div. of Essex Wire Corp.	Mansfield, Ohio	99934	Renbrandt, Inc.	Boston, Mass.
83501	Gavitt Wire and Cable Co. Div. of Amerace Corp.	Brookfield, Mass.	93632	Waters Mfg. Co.	Culver City, Calif.	99942	Hollman Electronics Corp. Semiconductor Div.	El Monte, Calif.
83594	Burroughs Corp. Electronic Tube Div.	Plainfield, N. J.	93929	G. V. Controls	Livingston, N. J.	99957	Technology Instrument Corp. of Calif.	Newbury Park, Calif.
83740	Union Carbide Corp. Consumer Prod. Div.	New York, N. Y.	94137	General Cable Corp.	Bayonne, N. J.			
83777	Model Eng. and Mfg., Inc.	Huntington, Ind.	94142	Phelps Dodge	Yonkers, N. Y.			
83821	Loyd Struggs Co.	Festus, Mo.	94144	Raytheon Co., Comp. Div., Ind. Comp. Operations	Quincy, Mass.			
83942	Aeronautical Inst. & Radio Co.	Lodi, N. J.	94148	Scientific Electronics Products, Inc.	Loveland, Colo.			
84171	Arco Electronics Inc.	Great Neck, N. Y.	94154	Wagner Elect. Corp., Tung-Sol Div.	Newark, N. J.			
84396	A. J. Gleesner Co., Inc.	San Francisco, Calif.	94197	Curtiss-Wright Corp. Electronics Div.	East Paterson, N. J.			
84411	TRW Capacitor Div.	Ogallala, Neb.	94227	South Chester Corp.	Chester, Pa.			
84970	Sarkis Tazian, Inc.	Bloomington, Ind.	94330	Wire Cloth Products, Inc.	Bellwood, Ill.			
85454	Bonnton Molding Company	Bonnton, N. J.	94375	Automatic Metal Products Co.	Brooklyn, N. Y.			
85471	A. B. Boyd Co.	San Francisco, Calif.	94682	Worcester Pressed Aluminum Corp.	Worcester, Mass.			
85474	R. M. Bracamonte & Co.	San Francisco, Calif.	94696	Magepccraft Electric Co.	Chicago, Ill.			
85650	Korfed Kords, Inc.	Hamden, Conn.	95023	George A. Philbrick Researchers, Inc.	Boston, Mass.			
85911	Seamless Rubber Co.	Chicago, Ill.	95236	Allies Products Corp.	Dania, Fla.			
86174	Fafnir Bearing Co.	Los Angeles, Calif.	95238	Continental Connector Corp.	Woodside, N. Y.			
86197	Clifton Precision Products Co., Inc.	Clifton Heights, Pa.	95263	Leecrall Mfg. Co., Inc.	Long Island, N. Y.			
86579	Precision Rubber Products Corp.	Dayton, Ohio	95265	National Coil Co.	Sheridan, Wyo.			
			95275	Vilamon, Inc.	Bridgewater, Conn.			
			95348	Gordos Corp.	Bloomfield, N. J.			
			95354	Hethode Mfg. Co.	Rolling Meadows, Ill.			

00015 48  
Revised October, 1969

From: FSC. Handbook Supplements

## SECTION VII OPTIONS, SPECIALS, AND MANUAL CHANGES

### 7-1. OPTIONS

7-2. No options are available at this time.

### 7-3. SPECIAL

7-4. A rear-mounted BNC connector may be added below the EXT GATE jack (J8). A chassis plug is normally installed in the J8 mounting hole as shipped from the factory.

7-5. Operation and parts for remote programming are shown in Section II. Schematic information for remote programming is shown in Section VIII.

### 7-6. MANUAL CHANGES

7-7. This manual applies directly to standard Model 5323A having serial prefix number 936 (refer to paragraph 1-7).

### 7-8. NEWER INSTRUMENTS

7-9. As changes are made, new instruments may have serial number prefixes not listed in this manual. The manuals for these instruments will be supplied with an added "Manual Change" sheet with the required information. If this sheet is missing contact your nearest Hewlett-Packard Sales and Service office, listed at the back of this manual.

### 7-10. OLDER INSTRUMENTS

7-11. To adapt this manual to 5323A with serial prefix number 924, make the following changes.

Tables 6-1 and 6-2,  
Change A16C1 to 1820-1962, C:FXD ELECT 9µF  
+50-10% 200 VDCW.

Figure 8-15,  
Change A16C1 from 15 µF to 9 µF.

7-12. To adapt this manual to 5323A with serial prefix number 908, make the following changes.

Tables 6-1 and 6-2,  
Change A16 to 05325-60039, POWER SUPPLY:  
+5.1V, +175V; 05325-20039, BOARD: BLANK  
P. C.

Add A16CR13: 1902-3139, DIODE BREAKDOWN:  
SILICON 8.25V, 5%.

Change A16R3 to 0683-5135, R:FXD COMP, 51K  
OHM, 5%, 1/4W.

Change A16R4 to 0683-2015, R:FXD COMP, 200  
OHM, 5%, 1/4W.

Delete A16Q3.

Figure 8-15,  
Replace with Figures 7-1 and 7-2.

THE FOLLOWING HP VENDORS HAVE NO NUMBER  
ASSIGNED IN THE LATEST SUPPLEMENT TO THE  
FEDERAL SUPPLY CODE FOR MANUFACTURERS  
HANDBOOK.

0000F	Malco Tool and Die	Los Angeles, Calif.
0000Z	Willow Leather Products Corp.	Newark, N. J.
000AB	ETA	England
000BB	Precision Instrument Components Co.	Van Nuys, Calif.
000CS	Hewlett-Packard Co., Colorado Springs	Colorado Springs, Colorado
000MM	Rubber Eng. & Development	Hayward, Calif.
000NH	A "N" D Mfg. Co.	San Jose, Calif.
000QQ	Coaltron	Oakland, Calif.
000WW	California Eastern Lab.	Burlington, Calif.
000YY	S. K. Smith Co.	Los Angeles, Calif.

Figure 7-1. Component Locators A16/A17

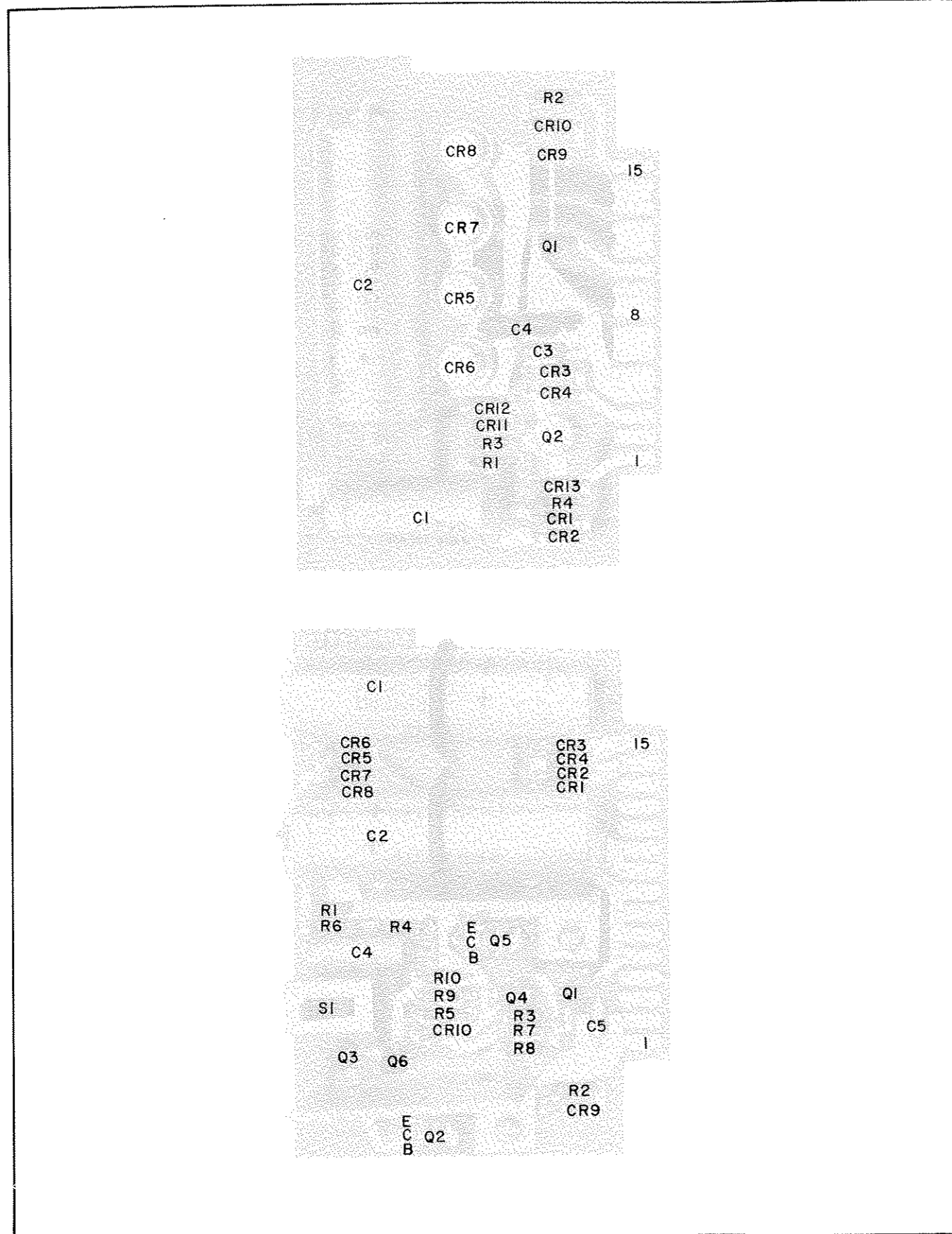
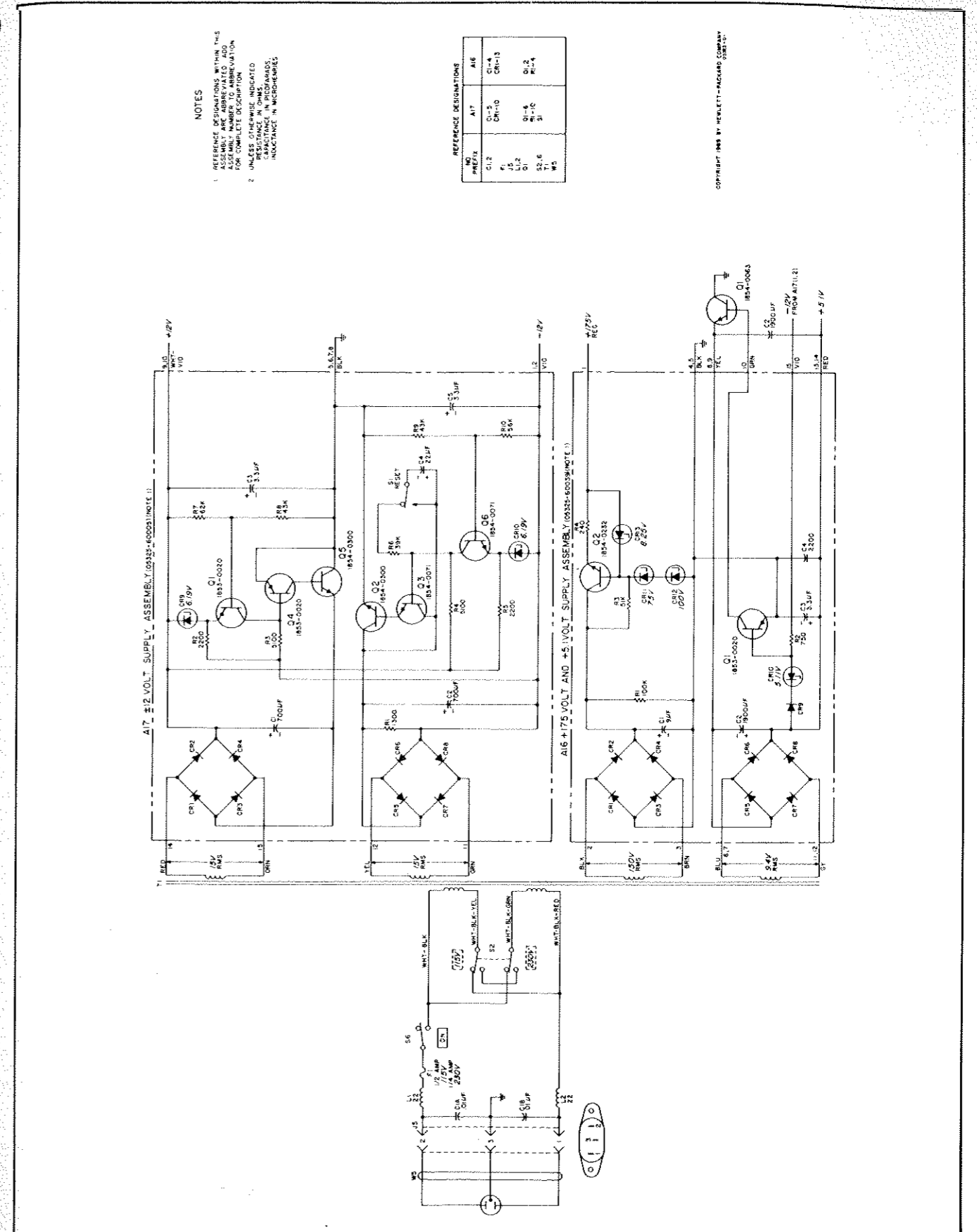


Figure 7-2. A16 +5.1V, +175V Power Supply; A17 ±12V Power Supply



## SECTION VIII CIRCUIT DIAGRAMS

8-1. This section contains the following:

a. General note for schematic diagrams in Figure 8-1.

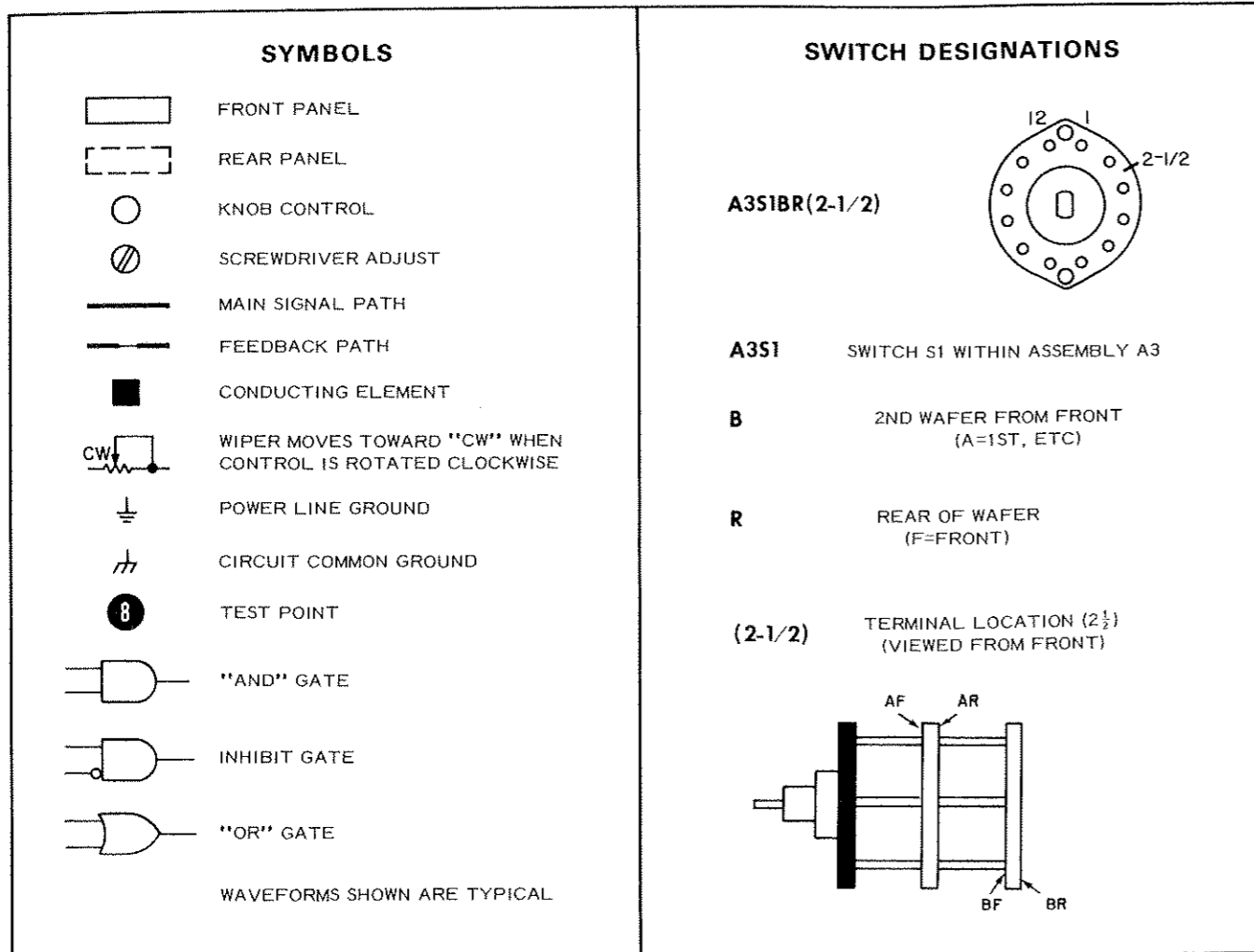
b. Flow diagram, Figure 8-2

c. Block diagram, Figure 8-3

d. Schematic diagrams and component locators for assemblies including theory of operation and troubleshooting procedures in Figures 8-4 through 8-15.

8-2. The diagrams, when unfolded, can be used with other parts of the manual or when tire manual is closed.

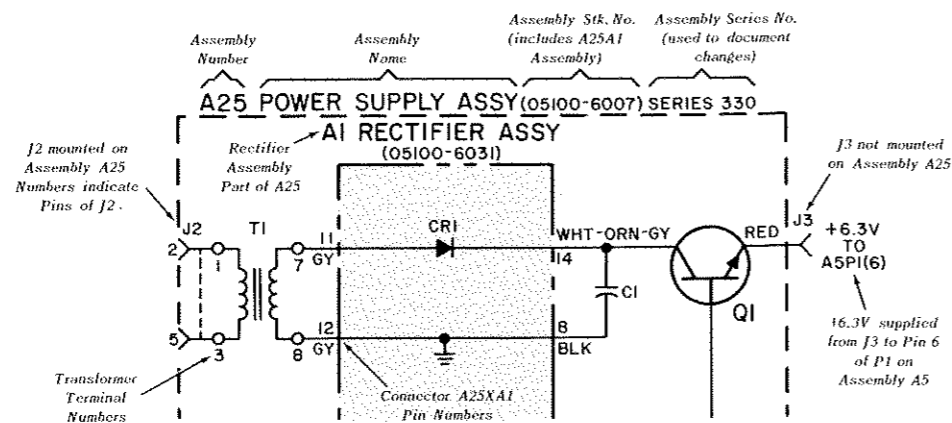
Figure 8-1. Schematic Diagram Notes

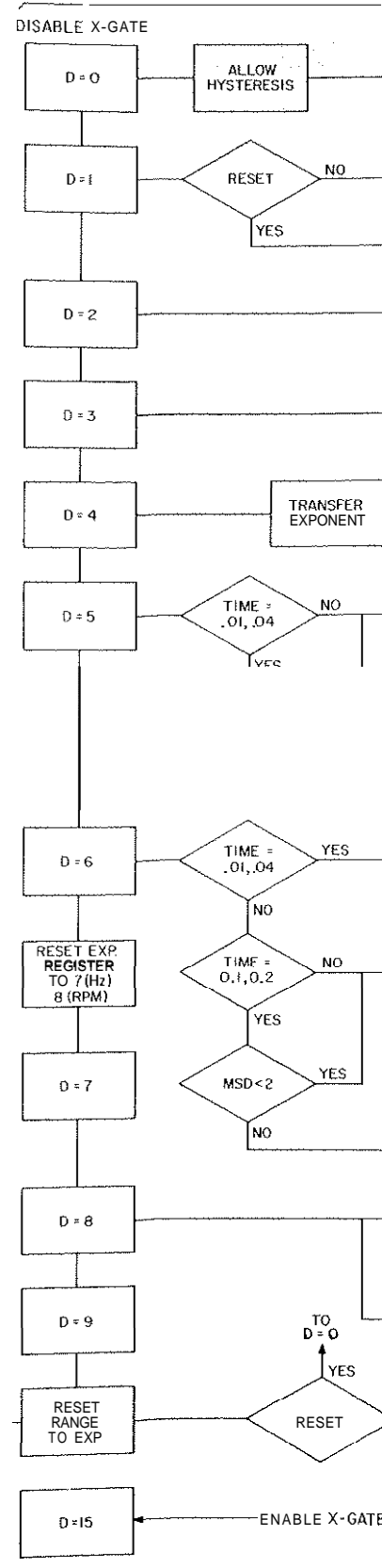
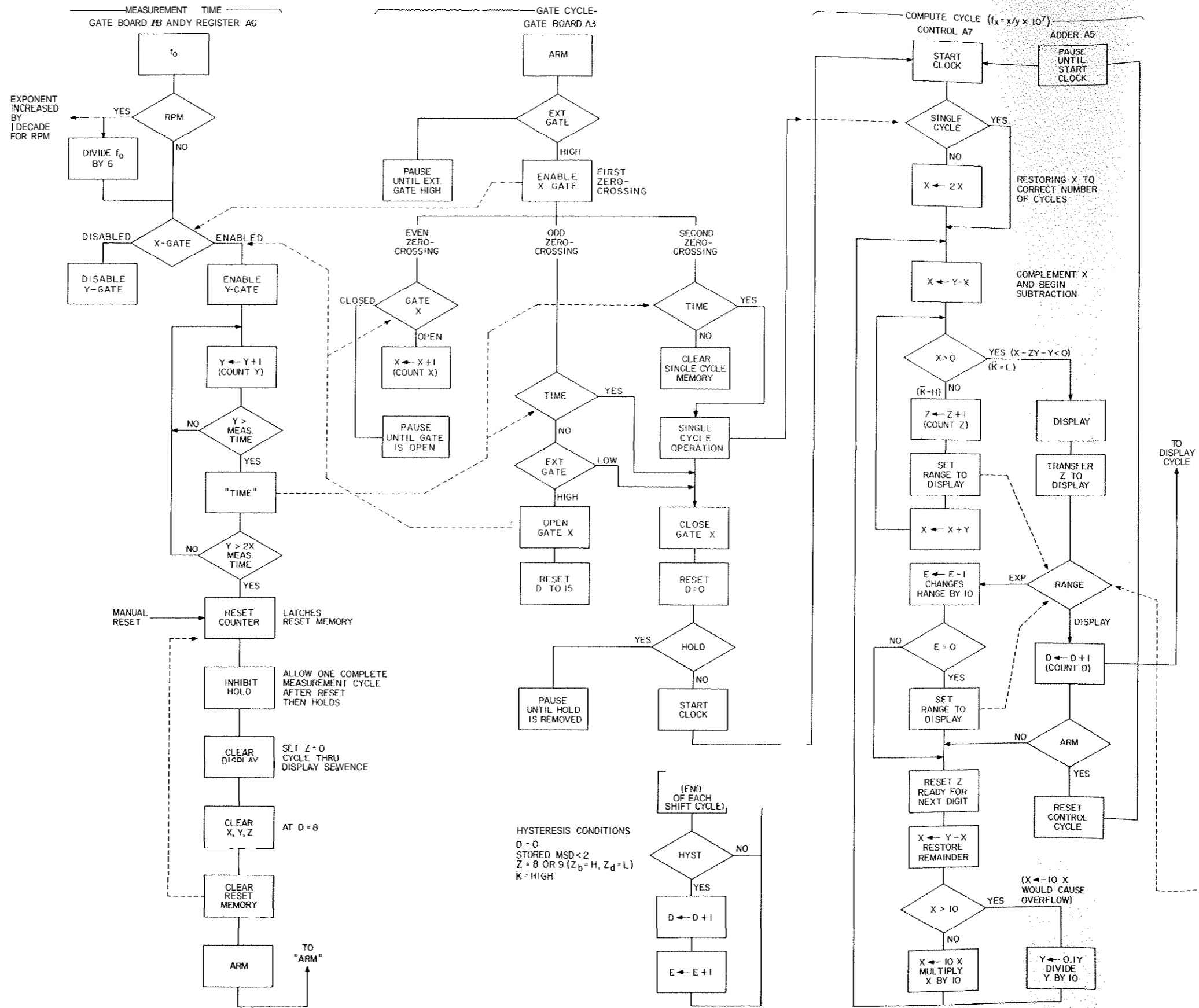


REFERENCE DESIGNATIONS

REFERENCE DESIGNATIONS WITHIN ASSEMBLIES ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

ASSEMBLY	ABBREVIATION	COMPLETE DESCRIPTION
A25	C1	A25C1
A25A1	CR1	A25A1CR1
NO PREFIX	J3	J3





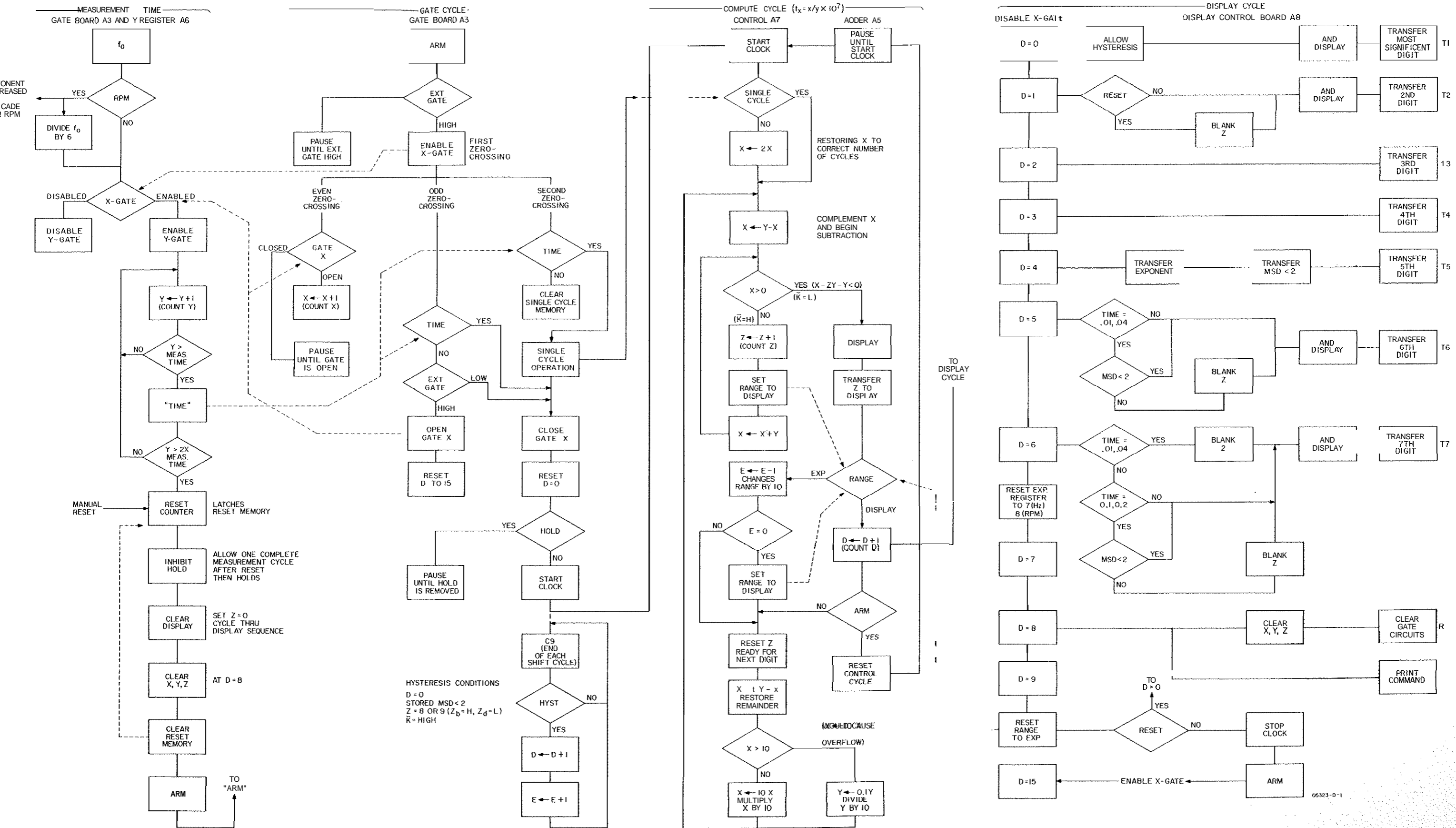


Figure 8-2. Flow Diagram

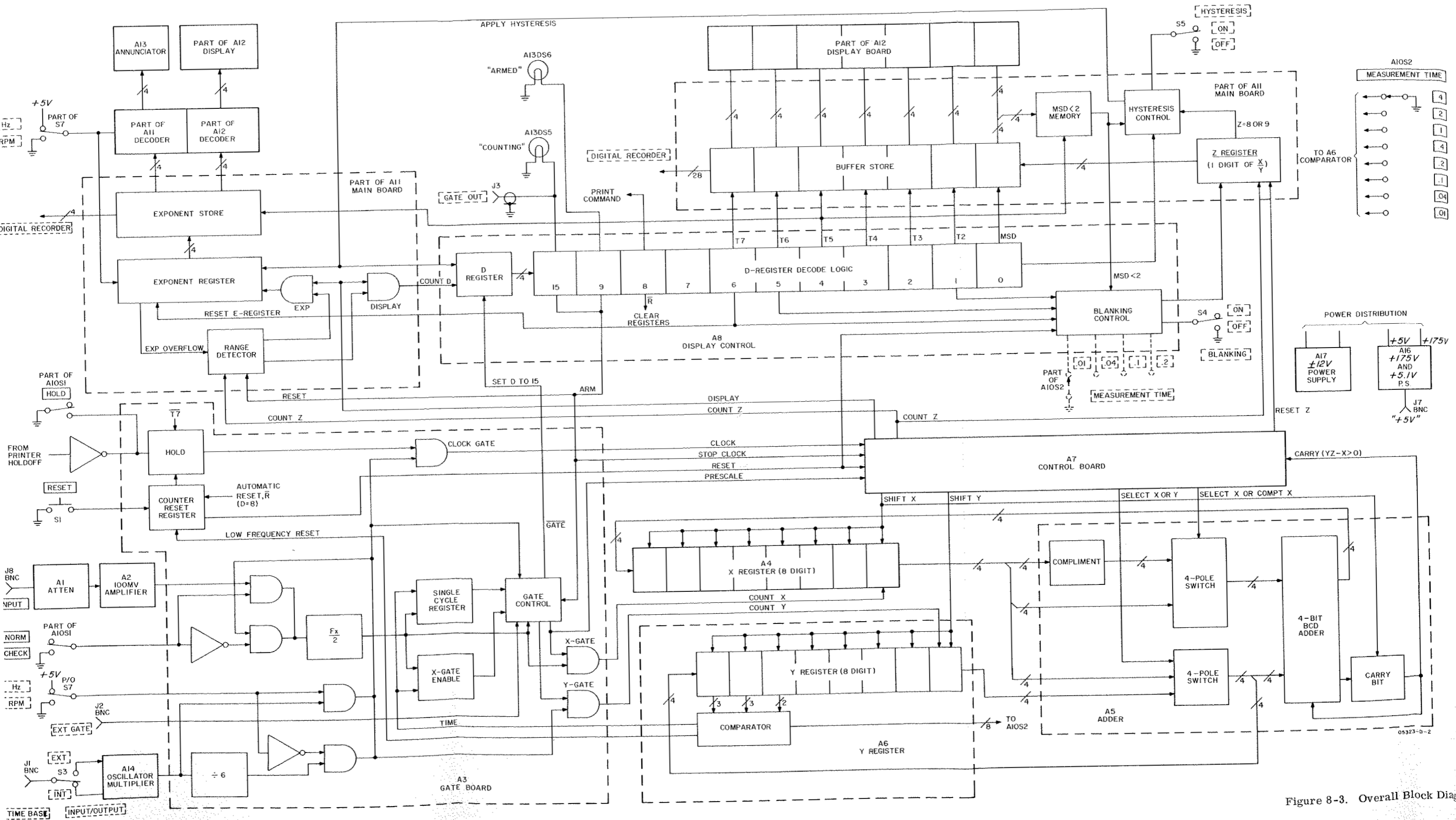


Figure 8-3. Overall Block Diagram



A1 OPERATION

The Counter input from J1 will be either AC- or DC-coupled to the attenuator depending on the position of S1. S2 selects the desired attenuation factor of 1, 10, or 100. Capacitors C2, C3, and C4 compensate for changes in frequency response as S2 is varied. The output of S2 is connected to the input of A2 via A9.

A1 TROUBLESHOOTING

If assembly is not working, check other positions of ATTEN and AC-DC switches. When it has been determined what positions are not operating, the trouble may be traced to the specific resistor, capacitor, or switch.

A2 OPERATION

The input signal from A1 appears at the gate of FET A. Q1A and Q1B control the gain of a differential amplifier composed of Q2, Q3, and Q4. The outputs from the differential amplifier are determined by the input signal level and the LEVEL control, R1-S7. The outputs appear as inputs to be differential Schmitt trigger, composed of Q5, Q6, and Q7. As the input signal level varies with time, the output of the differential amplifier will vary, which causes triggering of the differential Schmitt trigger. This output triggers a one-shot, composed of Q8-Q11. The output of A2 will be a pulse train from the one-shot that accurately follows the input signal, if the LEVEL control is set to allow triggering to occur. The output is connected to the input of A3.

A2 TROUBLESHOOTING

The first thing to do is check all the dc voltages coming into the board (-12V at pins 6 and 13, +12V at pins 7 and 8, and +5.1V at pin 15). Now check input signal at pin 1 (should be at least 100 mVrms, .28V peak-to-peak). Make waveform checks to determine which stage is not operating. When trouble has been isolated to a stage, make voltage and resistance measurements.

A2 ADJUSTMENT

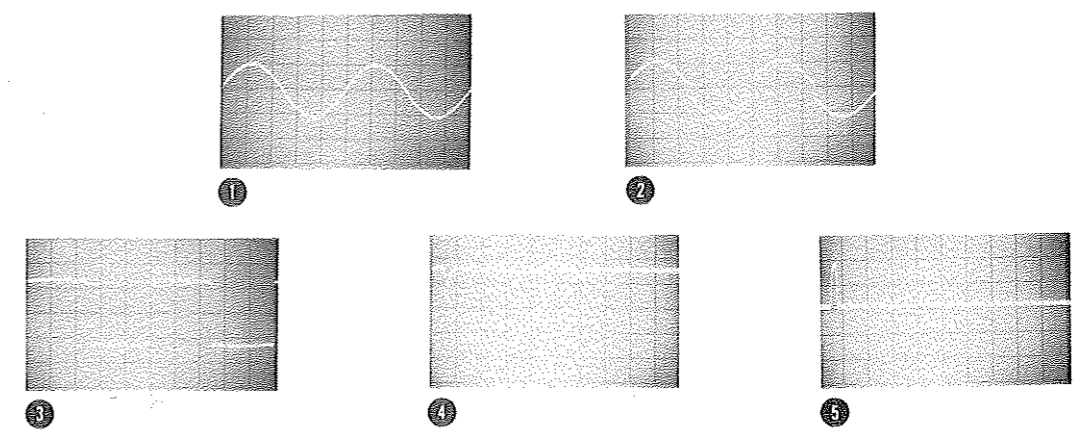
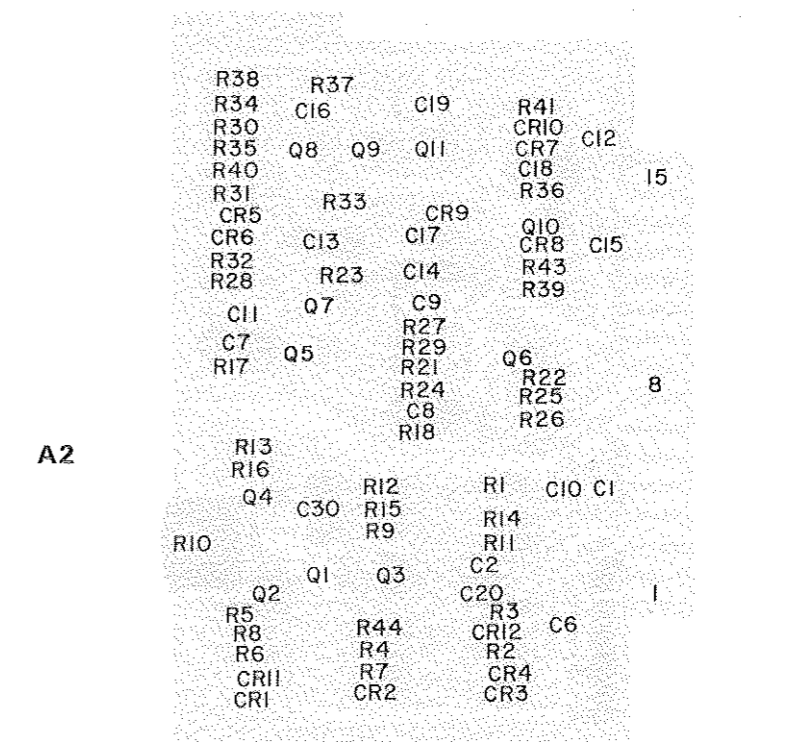
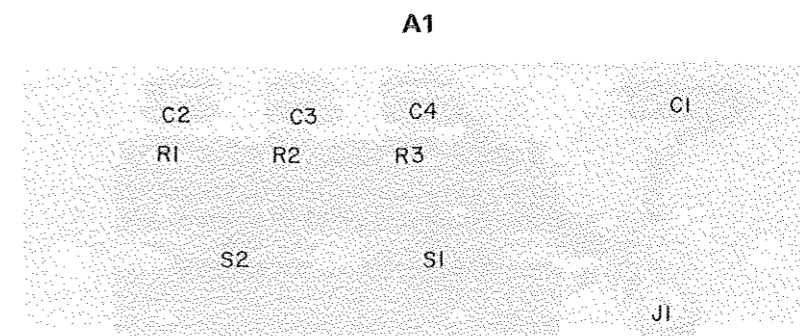
Follow procedure described in Table 5-4, ADJUSTMENTS (steps 1a through 1g), except use HP 651B Test Oscillator to supply 1 kHz input signal and HP 3400A RMS Voltmeter to monitor the input signal. Display should be approximately 1 kHz.

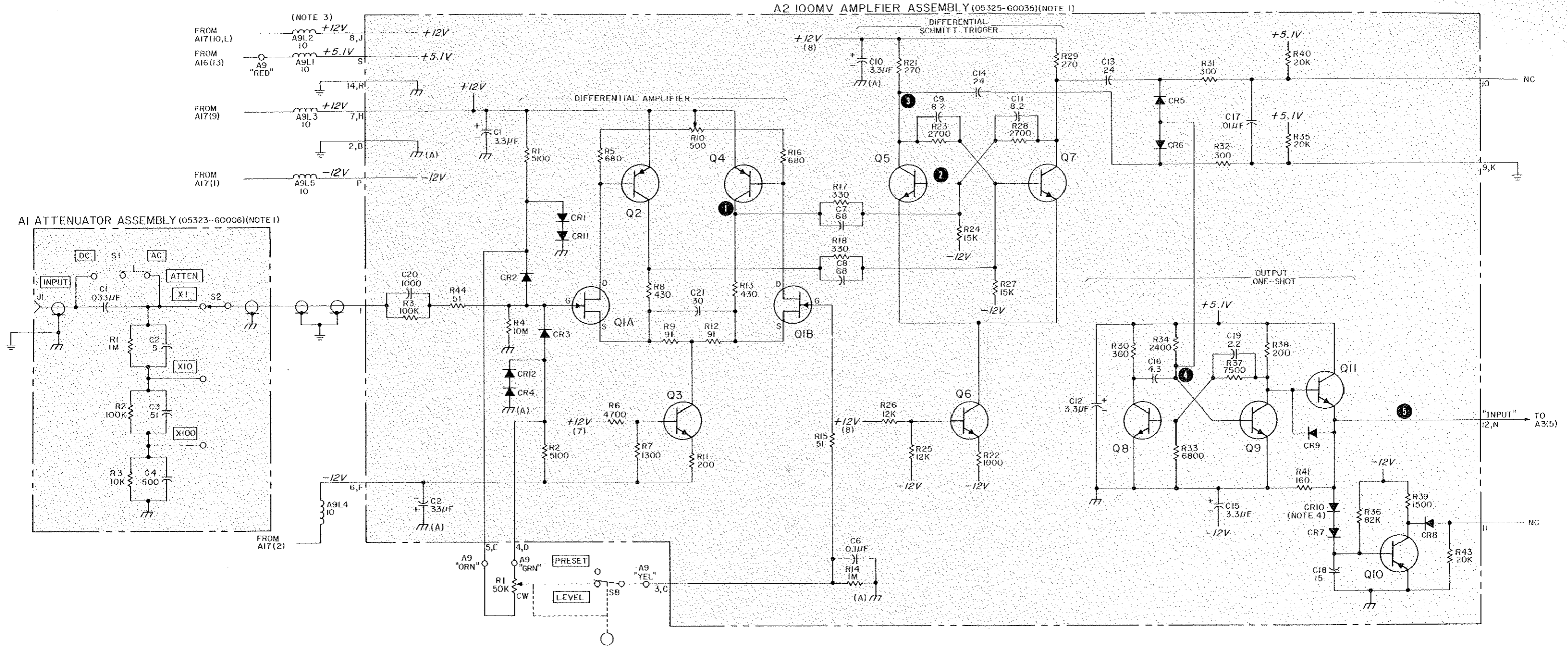
Set Controls:

POWER . . . . . ON  
MODE . . . . . NORMAL  
MEASUREMENT TIME . . . . . 4  
LEVEL . . . . . PRESET  
ATTEN . . . . . X1  
AC-DC . . . . . DC  
TIME BASE . . . . . INT  
Hz/RPM . . . . . Hz

All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, NP 1821A Time Base Plug-in, and HP 10004A 10:1 Probe.

WAVEFORM NO.	Oscilloscope Settings				
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM
1	.05V	x		x	.2 msec
2	.05V	x		x	.2 msec
3	.1V	x		x	.2 msec
4	.05V		x	x	.2 μsec
5	.2V		x	x	.2 μsec



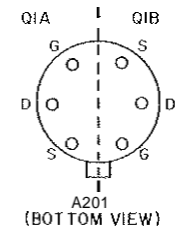


NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED RESISTANCE IN OHMS. CAPACITANCE IN PICOFARADS. INDUCTANCE IN MICROHENRIES
3. ALL CONNECTIONS TO XA2 ARE THRU A9, CONNECTOR HOARD ASSY
4. CR10 IS A 3 JUNCTION DIODE

REFERENCE DESIGNATIONS

NO PREFIX	A1	A2	A9
	CI-4	CI,2,6-21	
	J1	CR1-12	
R1	RI-3	Q1-11	
S8	SI,2	RI-18,21-41, 43,44	LI-5



TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
CR1, 4-6, 11, 12	1901-0040
2, 3	1901-0376
7-9	1910-0022
10	1901-0460
Q1	1855-0320
2, 4	1853-0015
3, 6	2N3640
	1854-0071
5, 7	1854-0019
8, 9, 11	1854-0009
	2N709
10	1853-0036
	2N3906

05323-0-4

Figure 8-4 A1 Attenuator Board Assy  
A2 Input Amplifier Assy  
8-7

### A3 OPERATION

IC1, IC9 and signal  $\overline{RPM}$  control the selection of either Hz or RPM as the basic Counter unit of measurement. Fy pulses are used for frequency measurement at the 10 MHz clock frequency; Fy pulses are divided by 6 in IC9 for RPM measurement.

IC2 (A, B, C), IC4B, and signal  $\overline{CHECK}$  control the selection of either NORM or CHECK mode. When  $\overline{CHECK}$  is HIGH, IC2B will be enabled, and IC2A will be disabled via IC4B. This condition allows Fx pulses to appear at the output of IC2C; the resultant pulses represent  $\overline{Fx}$  because of inversion in IC2C.

The Counter may be reset either manually or automatically. If the RESET pushbutton is momentarily depressed, the R input to the Reset flip/flop will become LOW, then HIGH, as the pushbutton is operated. This causes the CLEAR DISPLAY and RESET REGISTERS signals to go HIGH,  $\overline{RESET Z}$  to go LOW, and the Clock Gate to be enabled; IC5A, 6B, 7A, and 7B will be reset. The  $\overline{R}$  signal produced by A7 will then cause the CLEAR DISPLAY and RESET REGISTERS signals to go LOW and the  $\overline{RESET Z}$  signal to go HIGH. If the input to A3 disappears during a Gate cycle, the Reset flip/flop will produce a CLEAR DISPLAY signal which gives an all-zero Display. The gate flip/flops are reset by the  $\overline{R}$  signal which is generated near the end of the Display cycle (at D = 8).

If the  $\overline{HOLD}$  signal is LOW, a complete measurement cycle will occur until D = 6 when the trailing edge of the  $\overline{T7}$  signal will set the Hold Gate Control flip/flop, enable the Hold gate, and disable the Clock gate, preventing automatic reset.

After reset has been completed, an ARM signal from A8 will be generated causing IC8A1 to become HIGH. With no EXT GATE signal present, both inputs to IC8A will be HIGH resulting in IC8B4 going LOW. IC8B output must now become HIGH, which makes the J input of the Fx/2 flip/flop HIGH. The Fx/2 flip/flop is now armed, because the K input is always HIGH. The Fx/2 flip/flop will toggle on falling clock pulses as soon as Fx starts (rising Fx pulse produces falling clock input). Notice that if the EXT GATE input is LOW the J input of the Fx/2 flip/flop will also be LOW which prevents toggling. The states of critical gates and flip/flops after arming are shown in Table 8-1.

The first input pulse from A2 will cause the Fx/2 flip/flop to toggle. The X-Gate Enable flip/flop will change state to Q = L,  $\overline{Q}$  = H, and the PRESCALE and  $\overline{GATE}$  signals will go LOW. The next Fy pulse will enable the Y-Gate Control flip/flop and Y-Gate allowing COUNT Y pulses to occur. Each even input pulse will cause a COUNT X pulse to occur and the SC Register will change state.

When the TIME signal occurs, the Gate cycle will be terminated by the X-Gate Control flip/flop on the next odd input pulse. The X-Gate will be disabled (COUNT X = LOW), and the PRESCALE and  $\overline{GATE}$  signals will go HIGH. The next Fy pulse will disable the Y-Gate Control flip/flop and Y-Gate, which makes the COUNT Y = LOW. A special case arises when the TIME signal occurs before the second input pulse (Single-Cycle operation). The SC Control gate output IC4D13 will go LOW which prevents the SC Register from changing state on the 2nd input pulse, so a COUNT X = HIGH pulse will be generated, and  $\overline{GATE}$  will go HIGH, but PRESCALE will remain LOW.

After arming, IC8A1 will be HIGH. If the EXT GATE signal is held LOW, IC8A3 will be HIGH, which results in the output of the Fx/2 Control gate (IC8B6) going LOW. The J input of the Fx/2 flip/flop will be held LOW, and toggling will be inhibited (COUNT X and COUNT Y will remain LOW). When the EXT GATE signal goes HIGH, the J input of the Fx/2 flip/flop will go HIGH. The Gate cycle is now enabled.

If the EXT GATE signal becomes LOW during a Gate Cycle, the Fx/2 flip/flop (IC7B) will be inhibited from toggling. The EXT GATE Control gate output (IC8D11) will become HIGH along with the D input to the X-Gate Control flip/flop. The Gate cycle will then terminate on the next odd input pulse.

### A3 TROUBLESHOOTING

Check the input +5 Vdc at pin 15, S. Check for presence of Fx and Fy signals at pins 5 and C. If a problem exists with the mode or Hz/RPM functions, use the HP 10525A Logic Probe to check the NORM/CHECK and Hz/RPM decode logic. If the HOLD mode is inoperative, use the Logic Probe to check signal HOLD, the Hold Gate Enable flip/flop, Hold gate, and Clock gate.

Depress and hold the RESET pushbutton. Verify that the  $\overline{R}$  and  $\overline{T7}$  waveforms are correct. Release the RESET pushbutton and set the MODE switch to CHECK and MEASUREMENT TIME switch to .01. Verify that the  $\overline{RESET Z}$  and RESET REGISTERS waveforms are correct. If manual reset does not occur, check the Reset flip/flop and CLEAR DISPLAY waveform. If reset and arming occur correctly, the states of critical gates and flip/flops should be the same as shown in Table 8-1.

Next, check the CLOCK, COUNT Y and COUNT X output waveforms (the CLOCK and COUNT Y waveforms are nearly the same). Verify that the PRESCALE and  $\overline{GATE}$  signals go LOW on the first Fx pulse.  $\overline{GATE}$  should go HIGH at the end of the Gate cycle. Check the external gate function by using the Logic Probe on signals ARM, EXT GATE, and IC8A, IC8B, and IC8D. This procedure should isolate the trouble to an individual gate element, flip/flop, or counter.

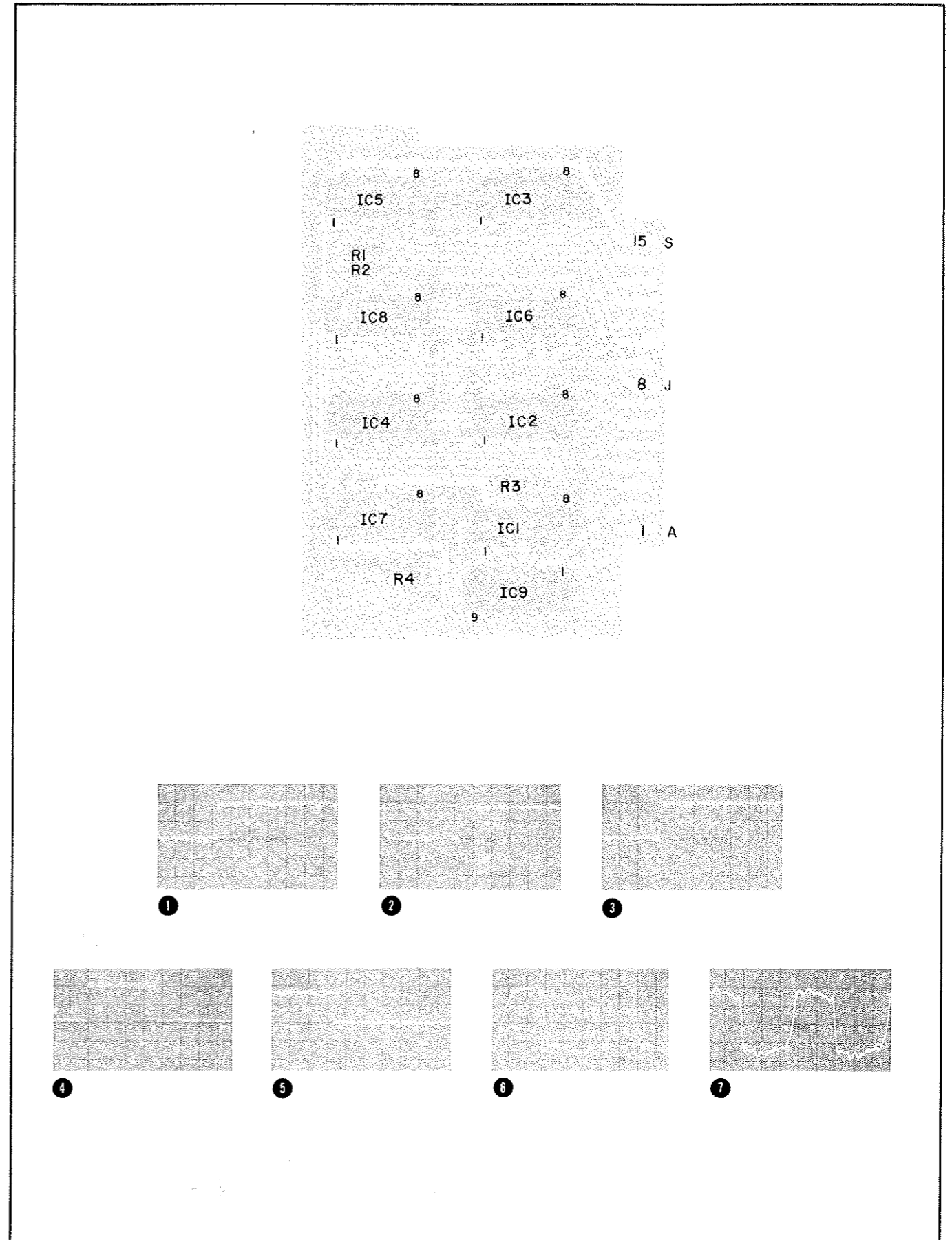
COUNTER SETTINGS

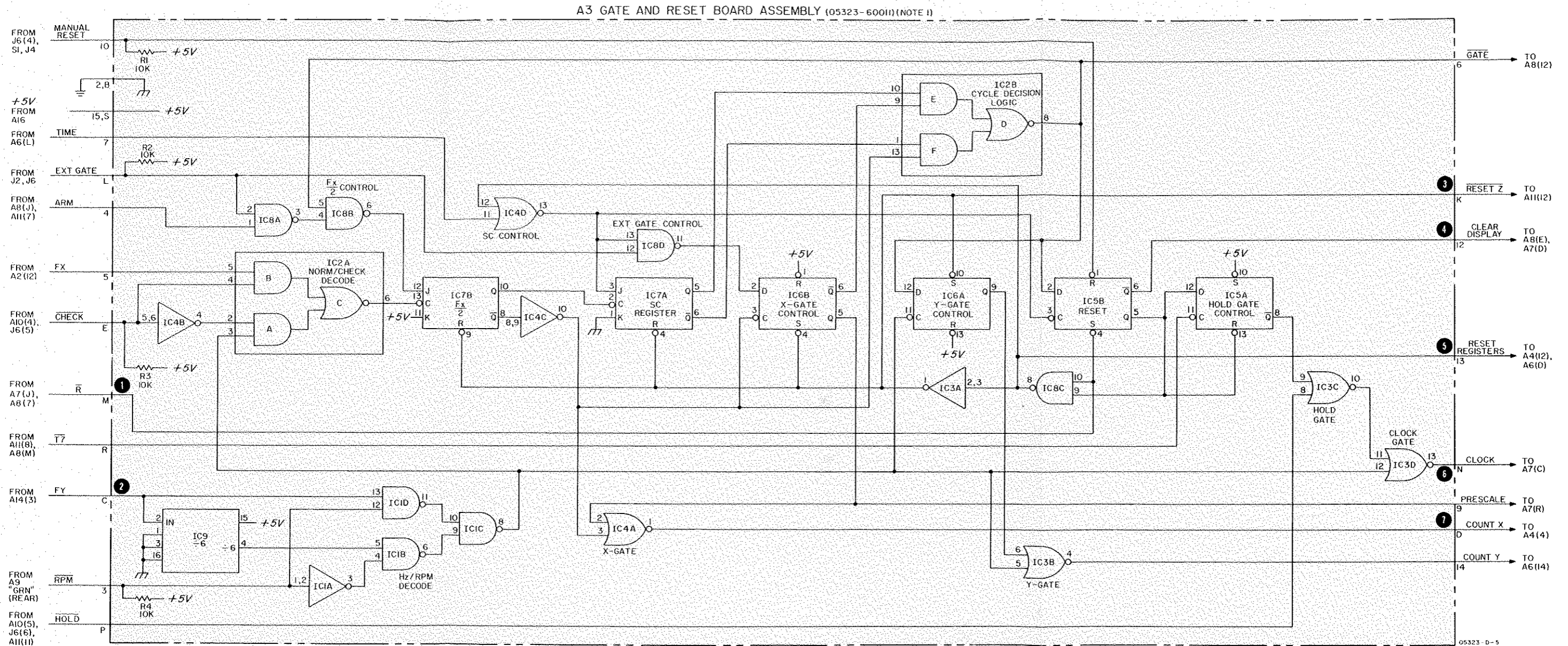
- A. RESET, . . . . . depress and hold  
 MODE . . . . . CHECK  
 MEASUREMENT TIME . . . . . .01  
 TIME BASE . . . . . INT
- B. MODE . . . . . CHECK  
 MEASUREMENT TIME . . . . . .01  
 TIME BASE . . . . . INT  
 Hz/RPM . . . . . Hz  
 BLANKING . . . . . ON
- C. RESET . . . . . depress and release  
 MODE . . . . . NORM  
 MEASUREMENT TIME . . . . . 4
- All waveforms taken with IIP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, IIP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

WAVEFORM NO.	COUNTER SETTINGS	V/CM	Oscilloscope Scplings				
			DC	SLOPE		SWEEP	
				+ -	/CM	MODE	
1	A	.2	x	x	.5 μs	NORM	
2	A	.2	x	x	.2 μs	NORM	
3	B	.2	x	x	5 μs	NORM	
4	C	.2	x	x	.2 μs	SINGLE	
5	B	.2	x	x	5 μs	NORM	
6	B	.1	x	x	20 ns	NORM	
7	B	.1	x	x	40 ns	NORM	

Table 8-1. A3 States (Counter Armed)

ELEMENT	DESIGNATION	STATES OR GATE OUTPUT
Fx/2 F/F	IC7B	J = H, Q = L, $\bar{Q}$ = H
SC Register	IC7A	J = H, Q = L, $\bar{Q}$ = H
X-Gate Control F/F	ICRR	D = L, Q = H, $\bar{Q}$ = L
Y-Gate Control F/F	IC6A	D = H, Q = H
Reset F/F	IC5B	D = H, Q = H, $\bar{Q}$ = L
Hold Gate Control F/F	IC5A	D = H, $\bar{Q}$ = H
Fx/2 Control Gate	IC8B	LOW
SC Control Gate	IC4D	HIGH
Ext. Gate Control	IC8D	LOW
Cycle Decision Logic	IC2 (D, E, F)	HIGH
X-Gate	IC4A	LOW
Y-Gate	IC3B	LOW
Hold Gate	IC3C	LOW
Clock Gate	IC3D	Enabled (Fy or Fy/6)





**NOTES**

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS.

**TABLE**

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC1,8	1820-0054
2	1820-0063
3,4	1820-0328
5,6	1820-0077
7	1820-0208
9	1820-0210

**REFERENCE DESIGNATIONS**

A3
IC1-9
RI-4

Figure 8-5. A3 Gate and Reset Board Assy

During reset, a RESET REGISTERS pulse is generated by A3. This pulse will reset all eight Decade Counter/Shift Registers (IC1-IC8). When COUNT X pulses appear at IC7(14) the first Decade Counter (IC7) will begin accumulating pulses. Overflow of the first Decade Counter produces a  $\pm 10$  output at IC7(3), which is counted by IC6. This process is repeated for successive counters, resulting in a capability of storing up to  $10^8$  COUNT X pulses.

During the Compute cycle, information from A5 must be periodically loaded into the X-Register. The data are loaded using summation lines  $\Sigma a$ ,  $\Sigma b$ ,  $\Sigma c$ , and  $\Sigma d$  which connect to Ia, Ib, Ic, and Id of IC8 (pins 1, 2, 7, and 8, respectively). The Z outputs of IC8 connect to the I inputs of IC1; the Z outputs of IC1 connect to the I inputs of IC2, etc. The 4-bit BCD words on the summation lines are shifted by  $\overline{\text{SHIFT X}}$  pulses into successive registers until, on the 8th  $\overline{\text{SHIFT X}}$  pulse, the first 4-bit BCD word is stored in IC7. The old data in the X-Register has been shifted, one digit at a time, into A5.

Buffer gates IC10A, B, C, and D develop signals Xa, Xb, Xc, and Xd corresponding to the 4-bit words stored in IC7. When  $\overline{\text{SHIFT X}}$  goes LOW, the Z outputs are enabled. Therefore, at the end of each  $\overline{\text{SHIFT X}}$  pulse (HIGH), a new 4-bit BCD word is available for use by A5. In order to maintain  $X > 10^7 = \text{LOW}$ , all 4 inputs to IC9A must be HIGH. Therefore, the Za, Zb, Zc, and Zd outputs from IC8 (pins 16, 15, 10, and 9, respectively) must be HIGH. The Decade counters use negative-logic, 1-2-4-8 coded outputs, so the Z outputs will be HIGH until IC1 overflows. When IC1 overflows, IC8(16) will become LOW, and  $X > 10^7$  will go HIGH.

A4 TROUBLESHOOTING

Check the  $i-5$  Vdc at pin 15, S. To check the count operation, set the MODE switch to CHECK and MEASUREMENT TIME to 4. Verify that COUNT X pulses are available at pin K. Then use the oscilloscope to trace the COUNT X overflow signal from pin 3 of each Decade Counter up to IC8. Verify that reset of the Decade Counters occurs with a Logic Probe and check the RESET REGISTERS waveform.

If the count operation is satisfactory, check the waveform of the  $\overline{\text{SHIFT X}}$  signal with MODE set to CHECK. The Z outputs of each Shift Register can then be checked with the oscilloscope to isolate a defective unit. Finally, check IC9A and the  $X > 10^7$  signal waveform.

Figure 8-5  
A3 GATE AND RESET BOARD ASSY

(See Page 8-9)

COUNTER SETTINGS

- A. MODE . . . . . CHECK  
MEASUREMENT TIME . . . . . .01  
TIME BASE . . . . . INT  
Hz/RPM . . . . . Hz
- B. MODE . . . . . CHECK  
MEASUREMENT TIME . . . . . 4  
TIME BASE . . . . . INT  
Hz/RPM . . . . . Hz

A12 OPERATION

IC1-IC7 are BCD to Decimal Decoders and Display Tube Drivers which receive the 4-bit BCD words from the Buffer Storage Registers in A11 and drive the display tubes. Refer to Section IV for the BCD to Decimal Decoder/Driver operating states (including blanked display). A LOW applied to pin 11 of display tubes DS2-DS7 will cause the decimal point to illuminate for the selected tube. Selection is controlled by

IC8, which receives inputs from the Exponent/Measurement Unit Decode Logic in A11. Table 8-6 in the discussion of the A11 Main Board Assembly shows the inputs to IC8. Using the Truth Table for the BCD to Decimal Decoder/Driver, together with the Decode Logic table, the operation of IC8 can be understood.

A12 TROUBLESHOOTING

Check the +175 Vdc at the WHT-RED push-on connector and the +5 Vdc at pin 21, Y. Ground the test point on the A11 Main Board with a clip lead and use the Logic Probe to check the inputs to the BCD to Decimal Decoder/Drivers (set MEASUREMENT TIME to 1 or 4). Use a DC Voltmeter to check the outputs of the Decoder/Drivers; enabled digit voltage should be approximately +2 Vdc and disabled digit voltage should be approximately +90 Vdc. The display tubes can be checked by substitution or interchanging.

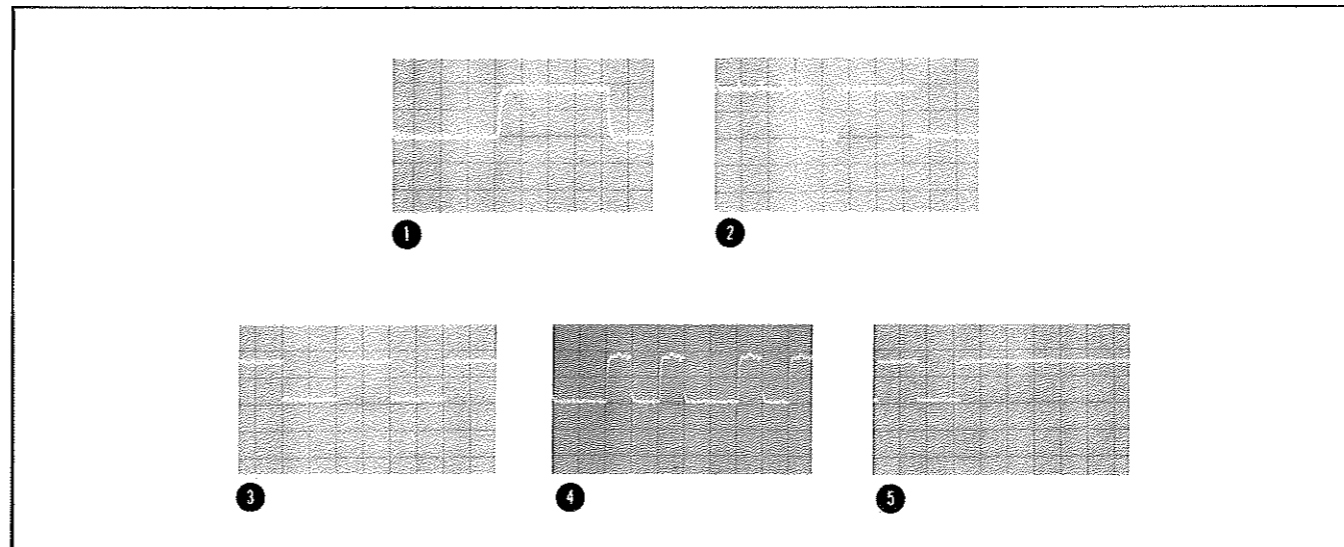
WARNING

USE EXTREME CAUTION WHEN TROUBLESHOOTING THIS ASSEMBLY AS +175 VOLTS IS PRESENT AT MANY POINTS ON BOARD.

All waveforms taken with HP 180A Oscilloscope, IIP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

WAVEFORM NO.	COUNTER SETTINGS	Oscilloscope Settings					
		SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM	MAIN TRIGGER
1	A	.2		x		.2 $\mu$ s	INT
2	A	.2		x	x	2 $\mu$ s	EXT(1)
3	B	.2		x	x	.1 ms	INT
4	B	.2		x		.4 $\mu$ s	EXT(2)
5	A	.2		x		10 $\mu$ s	INT

- (1) Connect external trigger input to  $\overline{\text{SHIFT X}}$ , IC8(13).
- (2) Connect external trigger input to Xa, IC10B4.



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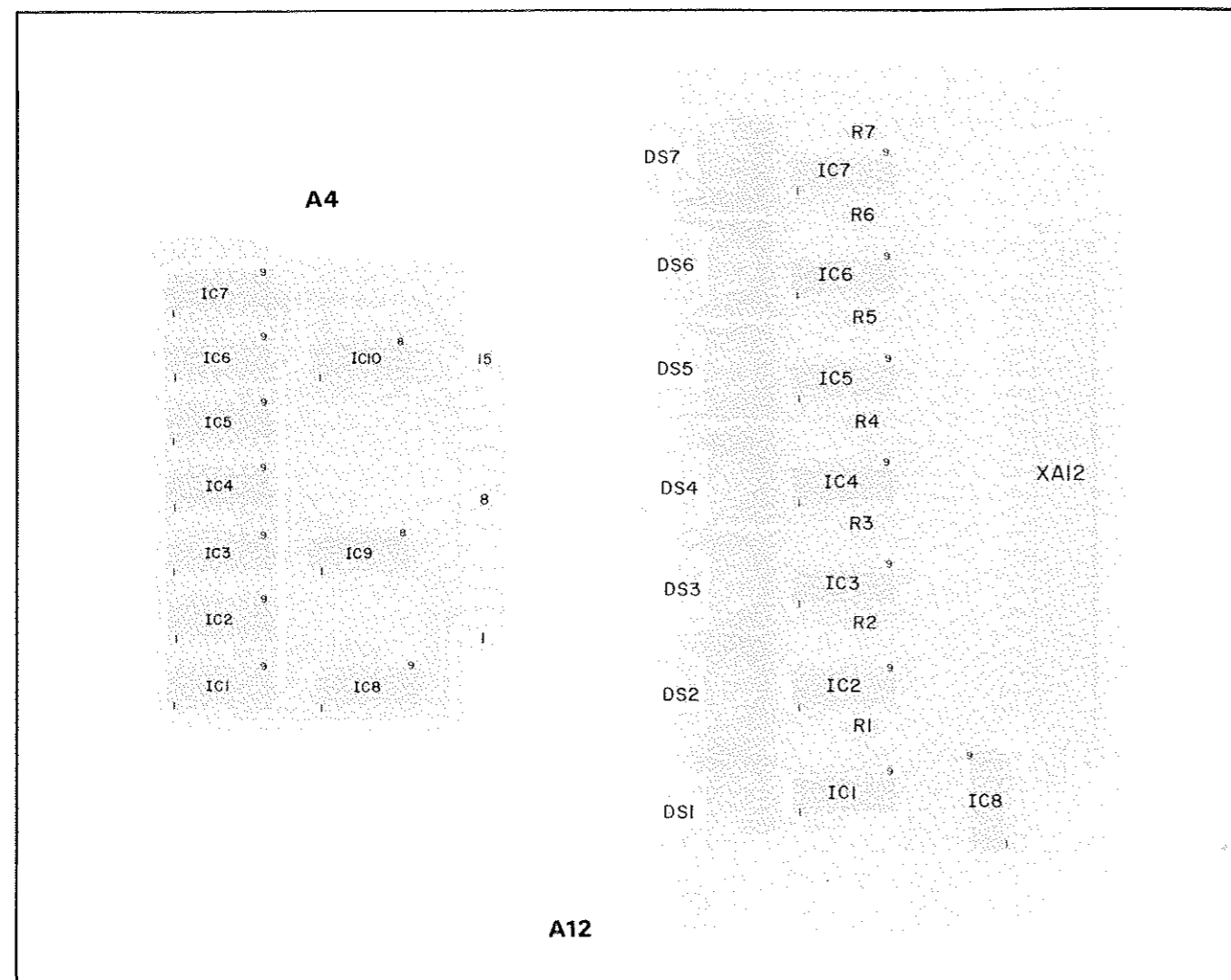
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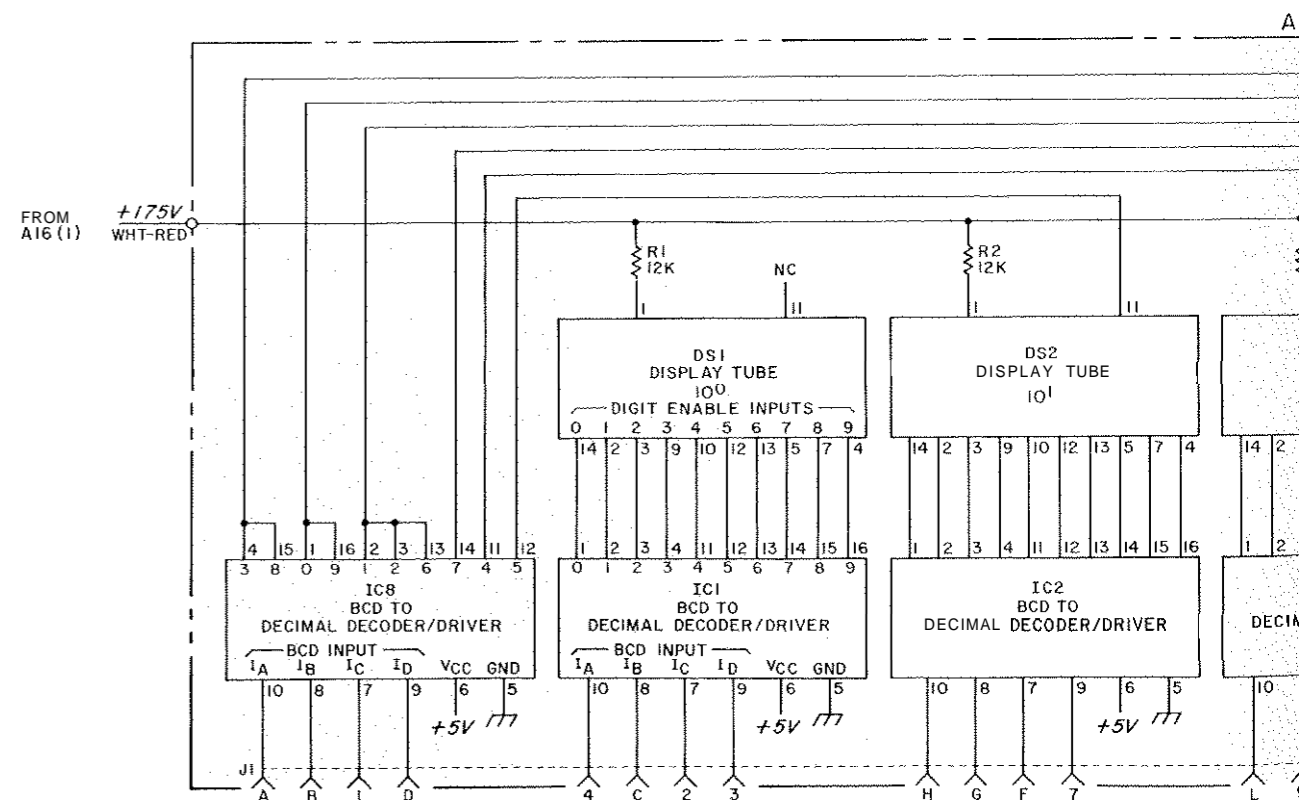
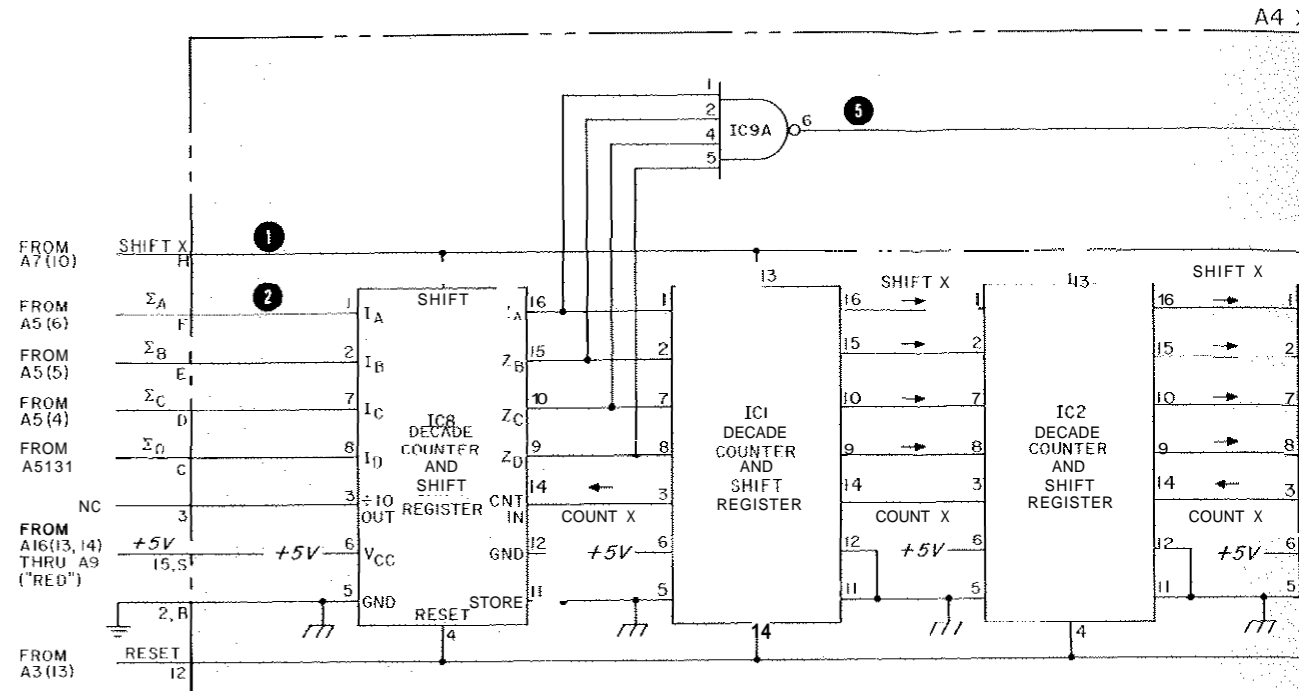
- REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
- UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS.

REFERENCE DESIGNATIONS	
A4	A12
IC1-10	DS1-7 IC1-8 R1-7

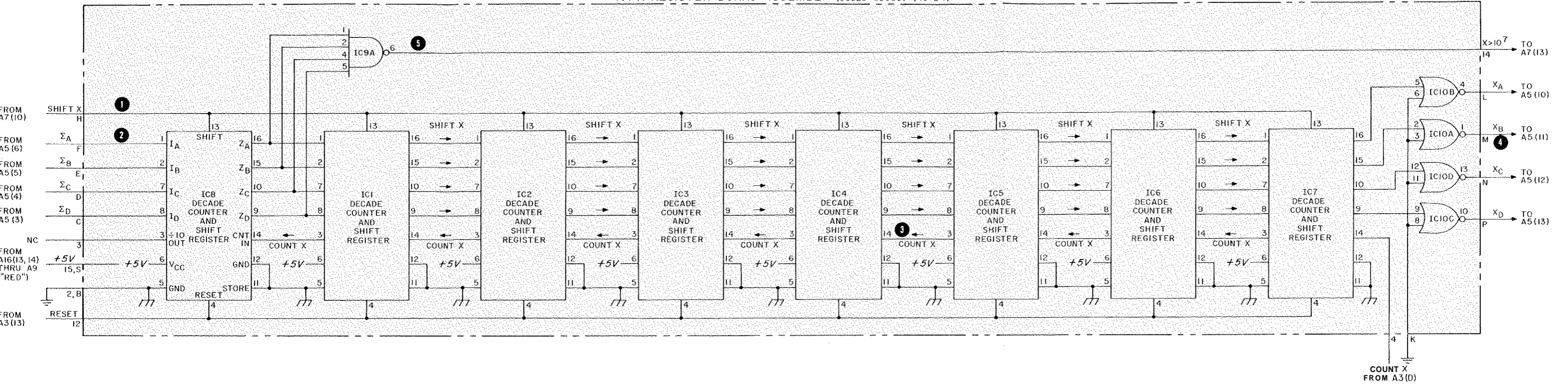
TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
A4 IC1-6,8 7 9 10	1820-0191 1820-0190 1820-0069 1820-0328
A12 IC1-8	1820-0092

05323-0-6



A4 X REGISTER BOARD ASSEMBLY (05323-60005) (NOTE 1)



A12 DISPLAY BOARD ASSEMBLY (05323-60008) (NOTE 1)

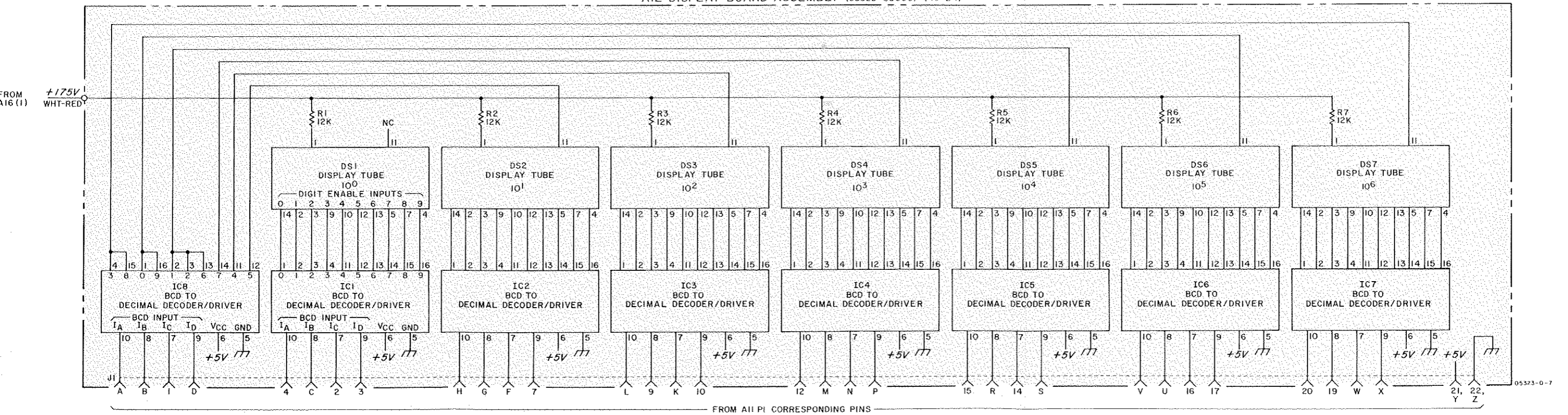


Figure 8-6. A4 X-Register Board Assy  
A12 Display Board Assy



At the start of the Compute cycle, the  $\overline{X+X}$  signal will be LOW, and both C1 and C2 are LOW ( $\overline{C2} = \text{HIGH}$ ). IC2C8 and IC2B6 outputs will be HIGH, and IC3C10 and IC3B4 outputs will be LOW. The first 4-bit BCD word stored in the X-Register will be gated via four-pole switches IC8 and IC6 to the A and B inputs of the 1st binary adder (IC5). The 1st binary adder (IC5) produces the sum and a C4 carry signal. If the sum is greater than 9, decode logic IC4(A, B, C), IC1D, and IC1A will cause IC1A1 to go LOW, which makes the B input word to the 2nd binary adder (IC7) equal to 6 in BCD form. The BCD 6 must be added to the A input ( $\Sigma$  output of 1st binary adder) when the sum is greater than 9, so that the  $\Sigma$  output of IC7 is in decimal form. A carry pulse will also be generated by the IC1A1 LOW output which appears at the D input of IC9A.

When the first  $\overline{\text{SHIFT X}}$  pulse occurs, the new least significant digit on the  $\Sigma a, \Sigma b, \Sigma c, \Sigma d$  lines will be loaded into the X-Register. On the trailing edge of the  $\overline{\text{SHIFT X}}$  pulse, the carry from IC1A1 will be clocked into IC9A. As a result of the C pulse, the Q output state of IC9A will be clocked into IC9B. The Q output of IC9B represents the carry-in to the 1st binary adder. A  $\overline{K}$  signal (carry pulse) will also be generated by IC9A ( $\overline{K} = \text{LOW}$  represents a carry pulse). The next 4-bit BCD word from the X-Register will now be summed and a carry-in will be added, if generated by the first summation.

At the end of a complete shift cycle, IC9 is reset ( $\overline{K} = \text{HIGH}$ ) by a  $\overline{C10}$  pulse. During the X + X operation,  $\overline{\text{SHIFT Y}}$  pulses are inhibited so that the Y-Register contents remain undisturbed.

The Xc + Y operation is the 2nd addition that occurs during a Compute cycle and represents the start of a division process. The  $\overline{X+X}$  and  $\overline{C2}$  signals are HIGH, and the C1 signal is LOW. IC2C8 and IC3B4 outputs will be HIGH, and IC3C10 and IC2B6 outputs will be LOW.

The first 4-bit BCD word stored in the Y-Register will be gated via four-pole switch IC8 to the A input of the 1st binary adder. The B input to the 1st binary adder should consist of the 9-complement of X, routed via four-pole switch IC6. To obtain the 9-complement of X, IC1B, IC1C, IC2A, IC3D, and IC4(D, E, F) are used. Table 8-2 shows the Boolean expressions and their simplified forms produced by the 9-complement logic. Adder operation is the same as that previously described for the X + X operation. The new Xc + Y word is shifted into the X-Register as X + X is shifted out.

Figure 8-6  
A4 X-REGISTER BOARD ASSY  
A12 DISPLAY BOARD ASSY  
(See Page 8-11)

Section VIII  
Diagrams

The third step in the Compute cycle is to add Y to the contents of the X-Register. This will be repeated until a  $\overline{K}$  signal is generated. At the start of this addition,  $\overline{C2}$  is LOW, so the IC3C10 output will be HIGH, and the IC3B4 output will be LOW.

The first 4-bit BCD word from the Y-Register will be routed by the IC8 four-pole switch to the A input of the 1st binary adder. The first word from the X-Register will be routed by the IC6 four-pole switch to the B input of the 1st binary adder. A sum and carry will be generated as previously described. The new sum (X + Y) will be stored in the X-Register.

When a carry signal ( $\overline{K} = \text{LOW}$ ) is generated, the A7 Control Board Assembly will cause C1 = LOW and  $\overline{C2} = \text{HIGH}$ , which initiates a new Xc + Y operation to restore the remainder of the last division, prior to multiplying by 10. After X has been multiplied by 10, a new division is started with Xc + Y being the first operation in A5.

A5 TROUBLESHOOTING

Check the +5 Vdc at pin 15, S. Check the Xa, Xb, Xc, Xd, and Ya, Yb, Yc, Yd input waveforms with the oscilloscope. Check the  $\overline{X+X}$ , C1,  $\overline{C2}$ , C,  $\overline{C10}$ , and  $\overline{\text{SHIFT X}}$  signal waveforms. Check the Ia, Ib, Ic, Id

waveforms to verify proper operation of IC8 (recirculation of Y for X + Y and Xc + Y operations). Compare the Xa, Xb, Xc, Xd waveforms to the A input to the 1st binary adder; they should be the same for the X + X operations.

Using the Logic Probe, check the operation of the Complement logic, using the data in Table 8-2; then check the B input to the 1st binary adder. Using the Logic Probe, check the operation of the +6 logic and the B input to the 2nd adder. To check the complement and +6 logic with the Logic Probe, the Counter should be in HOLD or ARMED (no signal input). Using a clip lead, various gate inputs can be made LOW by grounding them while the gate outputs are observed with the Logic Probe. Check the  $\Sigma a, \Sigma b, \Sigma c, \Sigma d$  output waveforms. Check the  $\overline{K}$  waveform with the oscilloscope and verify operation of the  $\overline{K}$  Memory flip/flops. The C signal (pin 14) can be used to sync the oscilloscope on non-repetitive waveforms.

COUNTER SETTINGS

MODE . . . . . CHECK  
MEASUREMENT TIME . . . . . .01  
TIME BASE . . . . . INT  
BLANKING . . . . . ON  
Hz/RPM . . . . . Hz

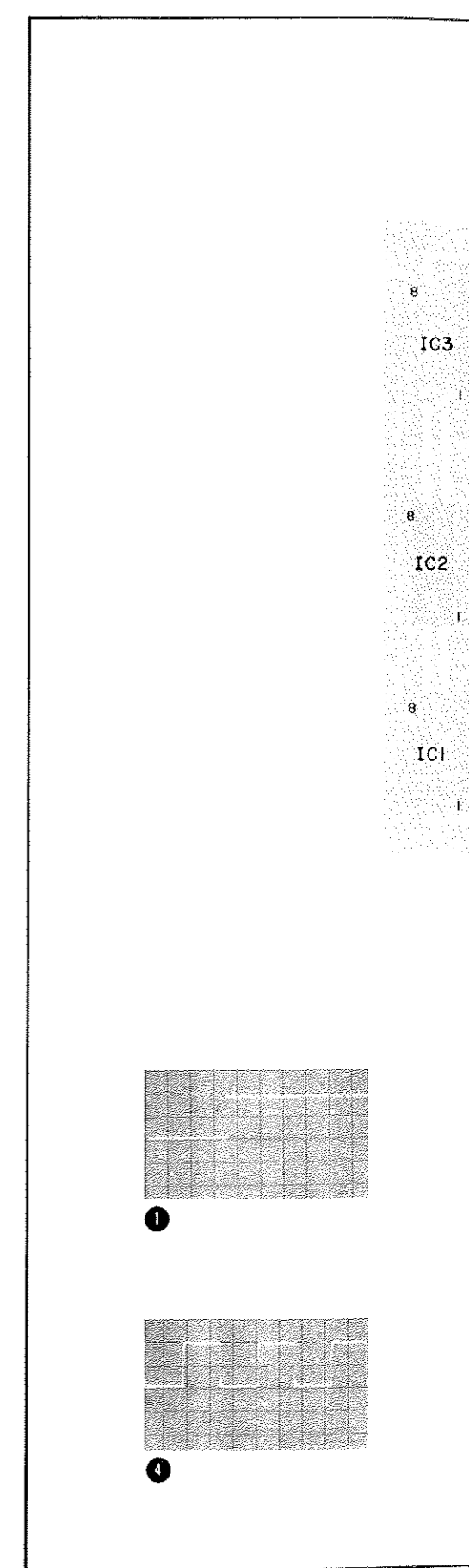
All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

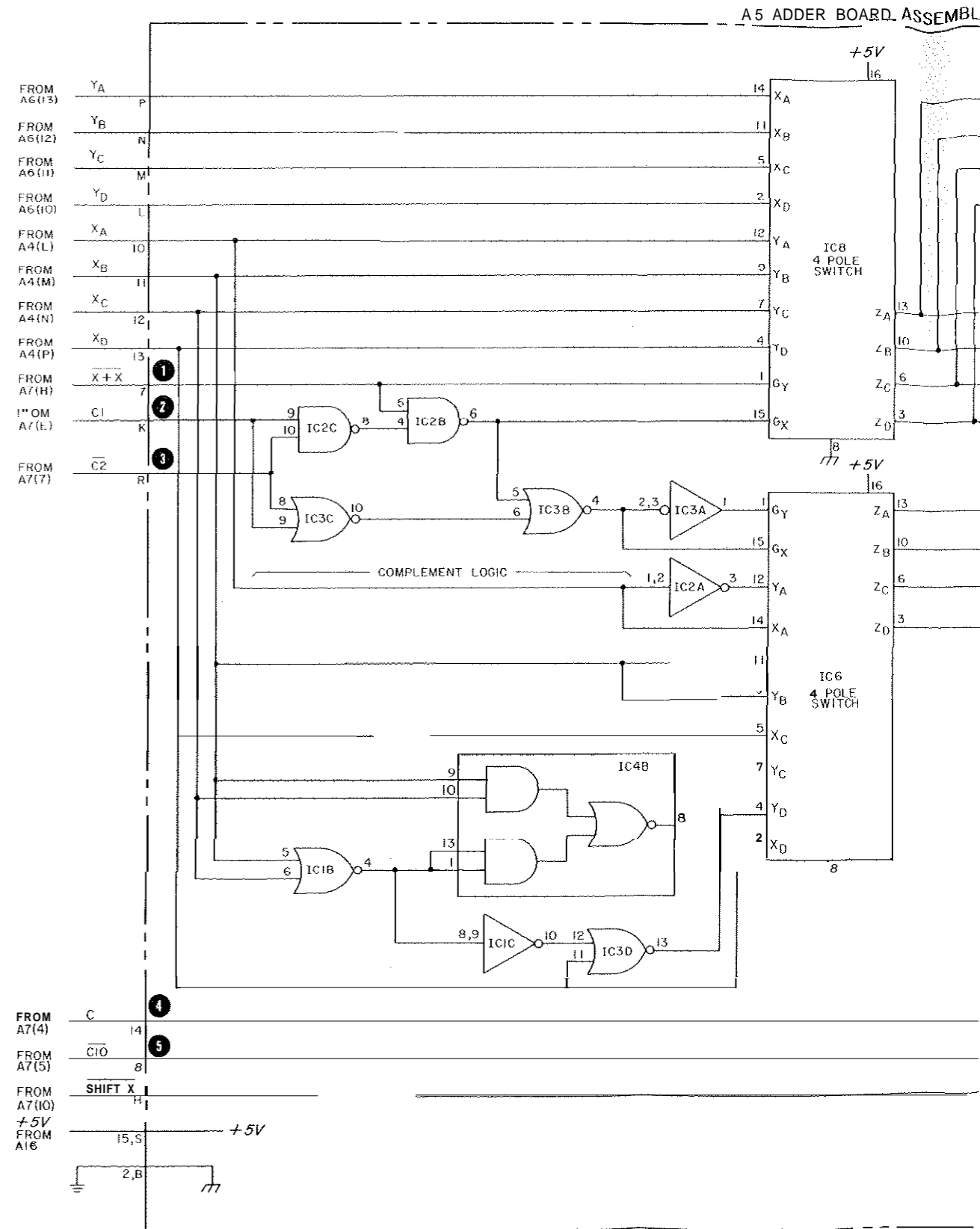
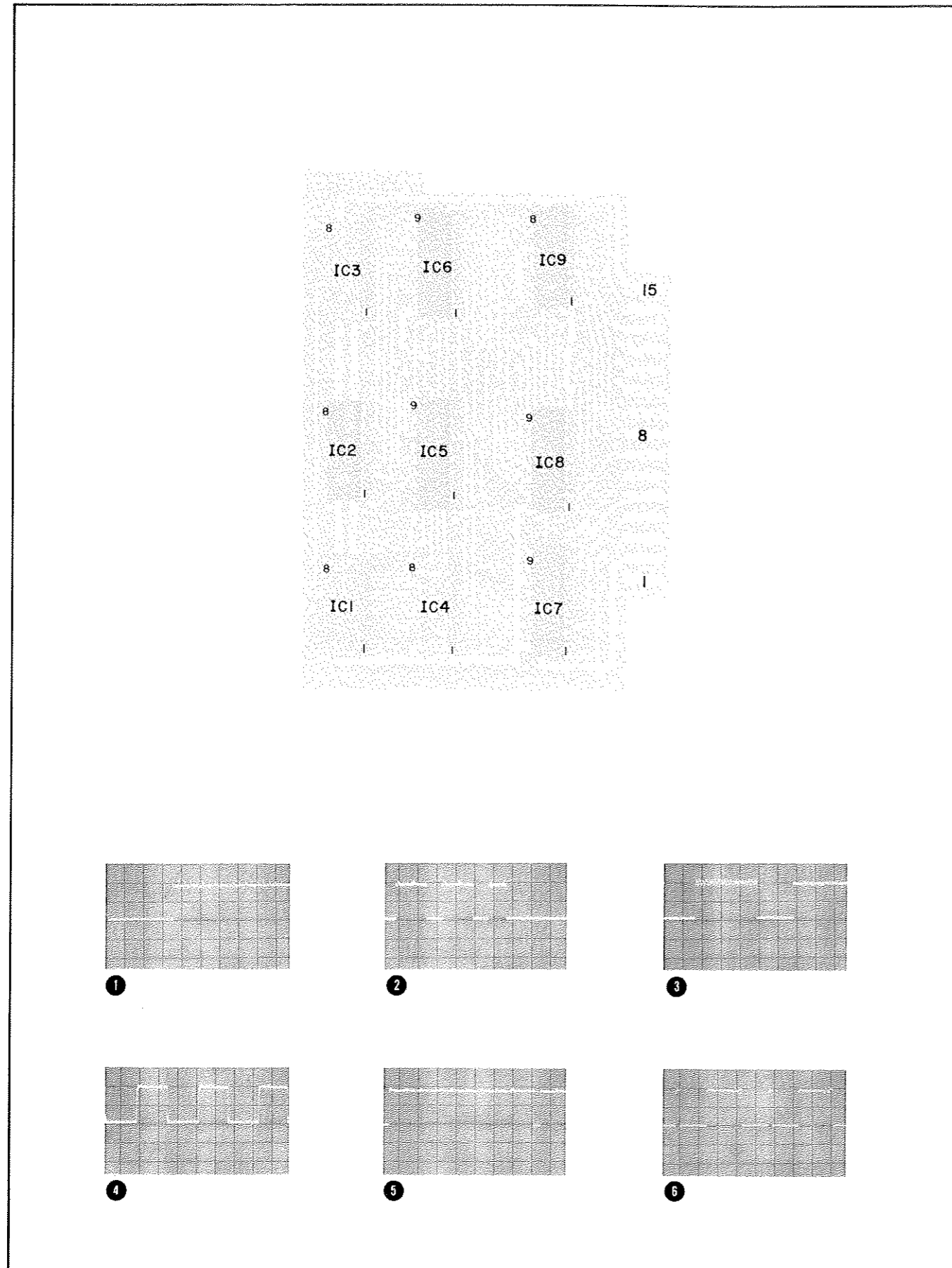
WAVEFORM NO.	Oscilloscope Settings					
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM	MAIN TRIGGER
1	.2		x	x	5 $\mu$ S	INT
2	.2		x	x	20 $\mu$ S	INT
3	.2		x	x	10 $\mu$ S	INT
4	.2		x	x	.5 $\mu$ S	INT
5	.2		x	x	2 $\mu$ S	INT
6	.2		x	x	10 $\mu$ S	EXT(1)

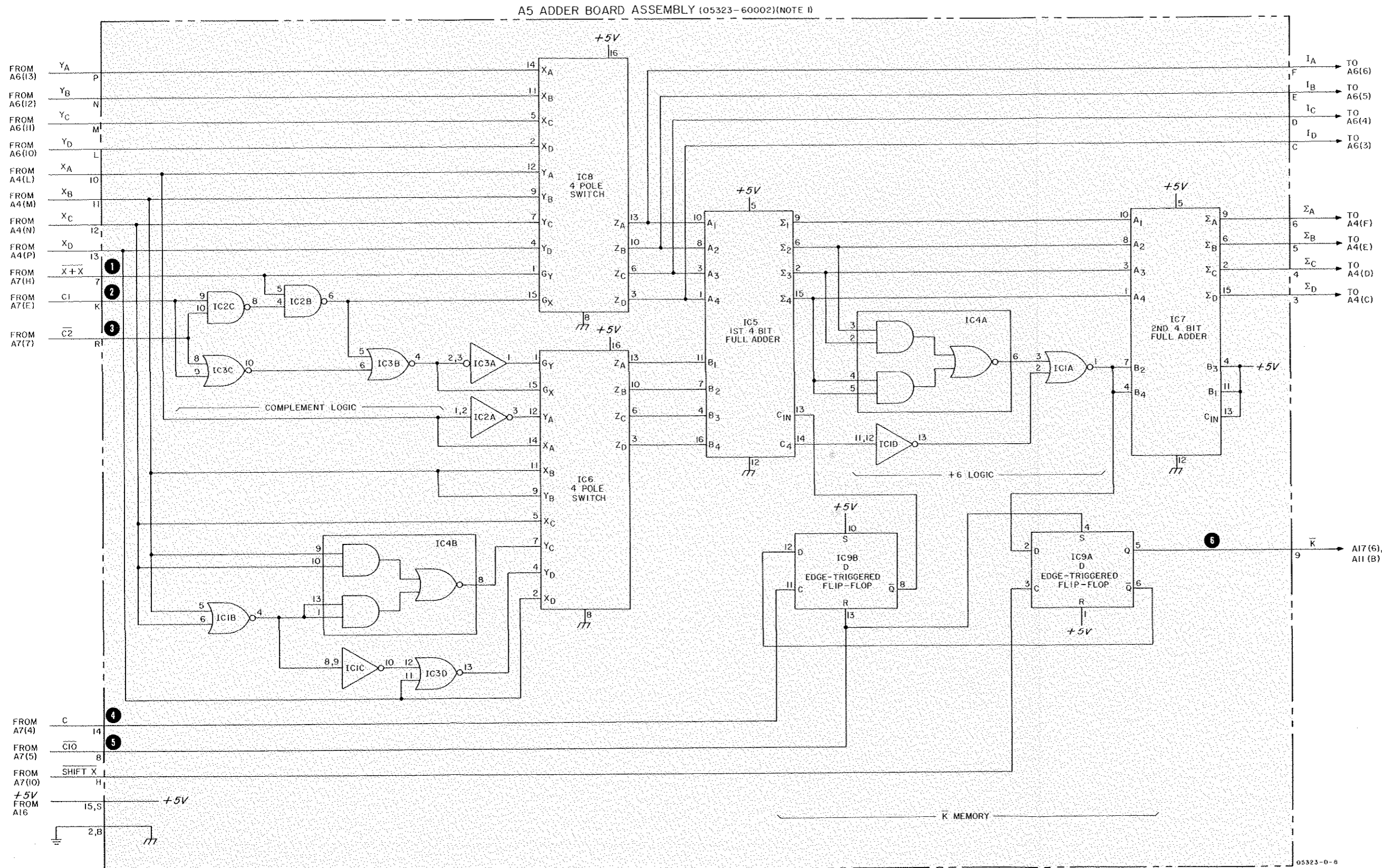
(1) Connect external trigger input to C signal, IC9B11.

Table 8-2. 9-Complement Logic Operation

INPUT	INPUT LOCATION	OUTPUT (B-INPUT TO 1ST BINARY ADDER)		OUTPUT LOCATION
		ORIGINAL EXPRESSION	SIMPLIFIED FORM	
Xa	A5(10)	$\overline{X1}$	$\overline{X1}$	IC6(13) IC5(11)
Xb	A5(11)	X2	X2	IC6(10) IC5(7)
Xc	A5(12)	$\overline{(X2 \cdot X4) + (\overline{X2} + X4)}$	$X2 \cdot \overline{X4} + \overline{X2} \cdot X4$	IC6(6) IC5(4)
Xd	A5(13)	$\overline{X8 + (\overline{X4} + X8)}$	$\overline{X4} + X8$	IC6(3) IC5(16)







NOTES

I. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC1, 3	1820-0328
2	1820-0054
4	1820-0063
5, 7	1820-0305
6, 8	1820-0135
9	1820-0077

REFERENCE DESIGNATIONS

A5
IC1-9

Figure 8-7. A5 Adder Board Assy

A6 OPERATION

Operation of the Y-Register is similar to the X-Register operation, previously described, except for an additional comparator circuit. COUNT Y pulses (Fy or Fy/6) appear at IC7(14) and are accumulated in the Decade Counters (IC1-ICE). This register also has a capability of storing 10<sup>8</sup> COUNT Y pulses. During the Compute cycle, SHIFT Y pulses shift the eight 4-bit BCD words into A5 via inverters IC12 (C, D, E, F) on lines Ya, Yb, Yc, and Yd. These words are re-circulated through A5 and loaded on lines Ia, Ib, Ic, and Id back into the Y-Register, preserving the contents of the register.

The MEASUREMENT TIME switch selects one of eight measurement times for gating Fx and Fy pulses: .01, .04, .1, .2, .4, 1, 2, or 4 seconds. The selected measurement time determines the states of one input of the 2-input NAND gates (IC9 and IC11). The other inputs of the NAND gates are controlled by the contents of the Y-Register (Z outputs of Decade Counters). The NAND gates compare the register contents to the selected measurement time, and the TIME signal will go HIGH when coincidence occurs (measurement time = number of COUNT Y pulses stored).

All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

WAVEFORM NO.	Oscilloscope Settings					
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM	MAIN TRIGGER
1	.2		x	x	2 μs	INT
2	.2		x	x	2 μs	EXT(1)
3	.2		x	x	20 μs	INT
4	.2		x	x		INT
5	.2		x	x		INT

(1) Connect external trigger input to SHIFT Y, IC8(13).

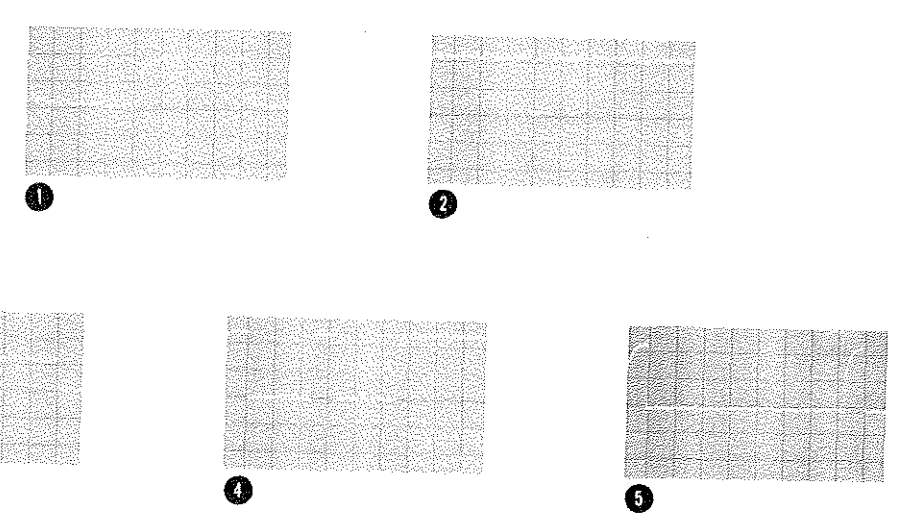
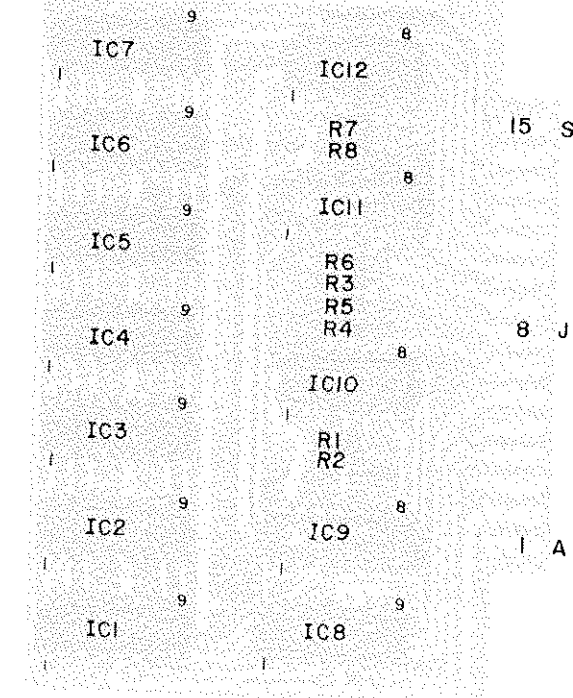
AG TROUBLESHOOTING

Check the +5 Vdc at pins 15, S. To check the count operation, verify that COUNT Y pulses are present at pin 14. Trace the COUNT Y signal through the counters by observing the waveform at the CNT IN (pin 14) terminals. To check the shift operation, verify that SHIFT Y, RESET REGISTERS, and Ia, Ib, Ic, Id signals are present. Trace the shifted data at the Z outputs of each shift register up to the output buffers. Check the Ya, Yb, Yc, Yd output waveforms.

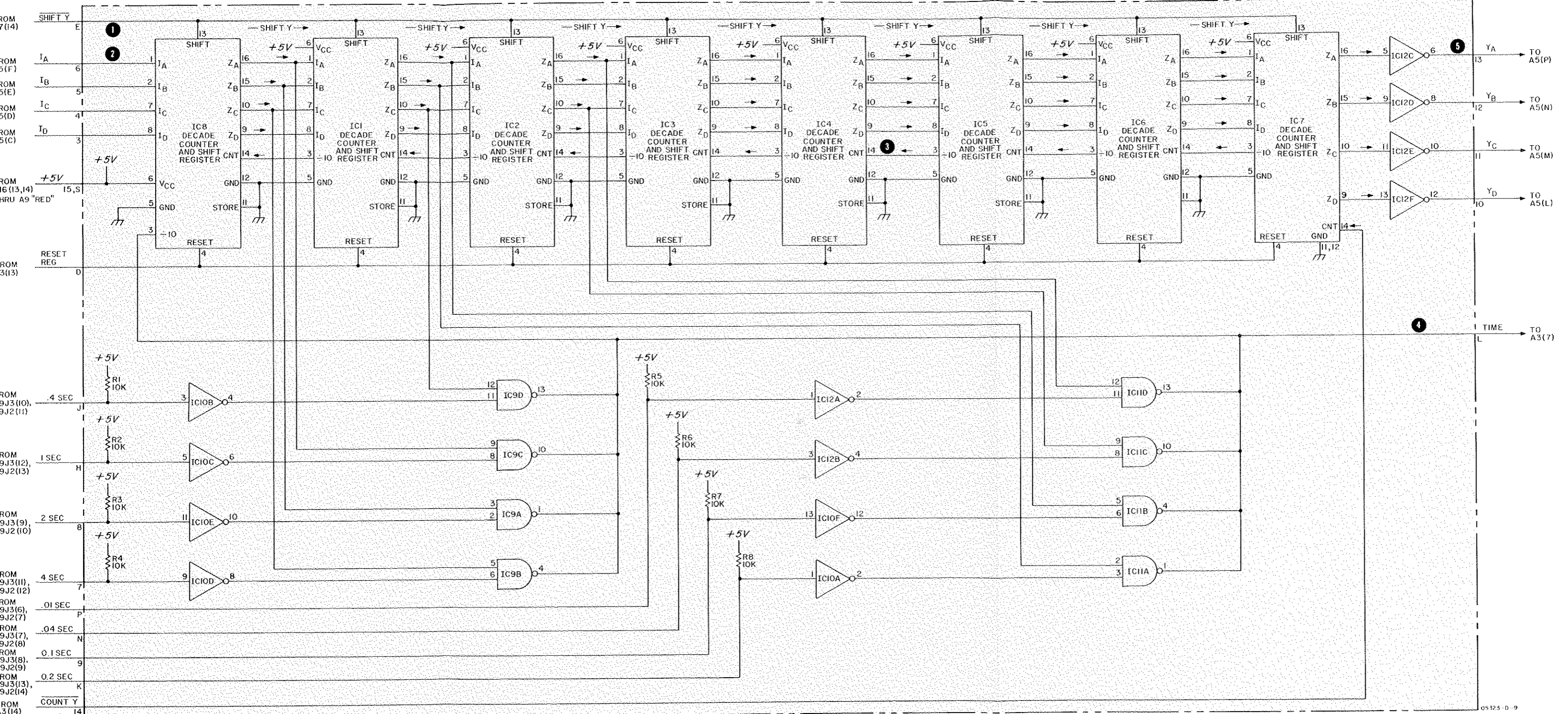
If count and shift operation are correct, check the comparator logic with the Logic Probe; then, check the TIME Signal waveform. This procedure should isolate the trouble to the defective counter/register or gate element.

COUNTER SETTINGS

MODE . . . . . CHECK  
MEASUREMENT TIME . . . . . 01  
TIME BASE . . . . . INT  
Hz/RPM . . . . . Hz  
BLANKING . . . . . ON



A6 Y REGISTER BOARD ASSEMBLY (05323-60003)(NOTE 1)



- NOTES**
1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
  2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS.

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC1-7	1820-0191
8	1820-0190
9,11	1820-0327
10,12	1820-0307

REFERENCE DESIGNATIONS

A6
IC1-12
RI-8

Figure 8-8 AG Y-Register Assy  
8-15

The  $\bar{R}$  signal generated during the Reset cycle will reset the C1 Register and set the C2 Register. When the Counter is armed,  $\bar{ARM}$  will go LOW which causes output IC3A1 to become HIGH, resetting IC1 and IC2 to all outputs HIGH. Additionally, the LOW  $\bar{ARM}$  signal will set the C1 Register and reset the  $X > 10^7$  and Restore X Registers. Gate inputs IC9B9, IC10B9, IC10A3, 5 and signal C1 will become LOW, and gate inputs IC9A5 and IC10B11 will become HIGH.

The PRESCALE signal will be HIGH until the second rising Fx transition, so gate input IC7D13 will be HIGH, and output IC7D11 will be LOW. Signal  $\bar{X} + \bar{X}$ , IC7A1, and IC4A1 will all become LOW. The LOW reset input to the C2 register will cause IC9B10, IC9A4, and signal C2 to become LOW, and IC10B10, IC10A4, and signal  $\bar{C}2$  to become HIGH.

The Fy (or Fy/6) clock pulses are divided by 16 in IC1 to produce a 625 kHz (or 625/6 kHz) internal computer clock. Ten pulses make up the subcycle for arithmetic operations: 8 shift pulses, C9, and C10. The 1st through 8th 625 kHz clock pulses produce 8 SHIFT X pulses (HIGH to LOW) at IC9C12, which shift the contents of A4 into A5. Input IC10C1 is LOW during this process, so no SHIFT Y pulses will occur. After the 8th SHIFT X pulse has occurred, the Za output of the 10-state Counter IC2(15) will go LOW. The LOW input at IC3B6 will disable IC9C, terminating SHIFT X pulses. The LOW input IC6D12, 13 produces a HIGH at IC6D11, which sets the C2 Register to Q = H,  $\bar{Q} = L$ ; C2 will go HIGH, and  $\bar{C}2$  will go LOW. At the 9th 625 kHz clock pulse, a C9 = HIGH pulse will occur. If a carry was produced by the first Xc + Y operation ( $\bar{K} = LOW$ ), the C1 Register would change state to Q = L,  $\bar{Q} = H$ , and C1 would go HIGH. When the tenth 625 kHz clock pulse occurs, the Za output of IC2 (pin 15) will become LOW and  $\bar{C}10 = LOW$  and DISPLAY = HIGH pulses will occur. If the  $X > 10^7$  signal is HIGH, the  $X > 10^7$  Register will change states to Q = L,  $\bar{Q} = H$ . If a carry pulse was not present at the C9 time, no DISPLAY pulse will occur, but a COUNT Z = LOW pulse will occur instead. The  $\bar{C}10$  trailing edge (LOW to HIGH) will cause the Restore X Register to change state ( $\bar{Q} = L$ ), which enables IC10C, allowing SHIFT Y pulses to occur during the next subcycle.

Figure 8-8

A6 Y-REGISTER ASSY

(See Page 8-15)

Section VIII  
Diagrams

In normal operation, the sequence of arithmetic operations is  $X + X$ ,  $Xc + Y$ ,  $X + Y$ . The  $X + Y$  operation is repeated until a carry signal ( $\bar{K} = LOW$ ) occurs. Each time the  $X + Y$  operation is completed without a carry signal a COUNT Z = LOW pulse will be generated by IC9A coincident with the C9 pulse. When  $\bar{K} = LOW$ , a DISPLAY pulse will be generated instead of COUNT Z. The  $\bar{K} = LOW$  signal also changes C1 to HIGH which causes the next operation to be  $Xc + Y$  (restore remainder). After the remainder has been restored the contents of the X-Register will be multiplied by 10 and the next display digit will be determined. The restored remainder can be multiplied by 10 either by eliminating the 8th SHIFT X pulse or supplying only one long SHIFT Y pulse. The method used will depend on the state of the  $X > 10^7$  signal. If the contents of the X-Register are  $> 10^7$ , the 8th SHIFT X pulse cannot be eliminated or the MSD would be lost.

Therefore,  $X > 10^7 = HIGH$  will set the  $X > 10^7$  Register to Q = H,  $\bar{Q} = L$ , and the previous carry pulse will reset the C1 Register to Q = L,  $\bar{Q} = H$ . The 1st 625 kHz clock pulse will cause SHIFT Y to go LOW. SHIFT Y will remain low until the 8th clock pulse when IC2(16) will go LOW, disabling IC10C. If the contents of the X-Register are  $< 10^7$ , the  $X > 10^7$  signal will remain LOW, and the  $X > 10^7$  Register will remain at Q = L,  $\bar{Q} = H$ . The previous carry pulse will reset the C1 Register to Q = L,  $\bar{Q} = H$  and the C2 Register to Q = L,  $\bar{Q} = H$ . When the D output of IC2(16) goes LOW at the end of the 7th SHIFT X pulse, gate input IC9C1 will go LOW, and SHIFT X will remain HIGH (no 8th SHIFT X pulse generated). Only 7 SHIFT X pulses will be generated.

When a single-cycle of Fx is measured (one COUNT X pulse), the PRESCALE signal will be LOW, so  $\bar{X} + \bar{X}$  will be HIGH during the 1st 8 SHIFT X pulses. Because  $X + X$  and  $\bar{C}2$  are HIGH, and C1 is LOW, the  $Xc + Y$  operation is the first one utilized by A5. In other words, Fx was not divided by two in A3; therefore, Fx was not multiplied by two during the Compute cycle. Instead, the division process is immediately initiated.

When the CLEAR DISPLAY signal goes HIGH, IC1 and IC2 will be enabled along with ICGA. DISPLAY pulses will be produced to clear the Display.

A7 TROUBLESHOOTING

Check the +5 Vdc at pin 15, S. Check the  $\bar{R}$ ,  $\bar{ARM}$  and CLEAR DISPLAY waveforms; using the Logic Probe, verify that the output signal states are as shown in Table 8-3 after reset and arming. Check the DISPLAY and COUNT Z waveforms with the MODE switch set to CHECK and MEASUREMENT TIME to .01. Check the other output waveforms. If reset and arming occur properly, but one or more output signals are incorrect, check the  $\bar{K}$ ,  $X > 10^7$ , and PRESCALE signals. If no output signals occur, check the CLOCK input and  $\div 16$  and Zd outputs from IC1; then, check the Za, Zb, Zc, Zd outputs from the 10-state Counter. This procedure should isolate the trouble to the defective gate element, register, or counter.

COUNTER SETTINGS

MODE . . . . .	CHECK
MEASUREMENT TIME . . . . .	.01
TIME BASE . . . . .	INT
Hz/RPM . . . . .	Hz
BLANKING.. . . .	ON

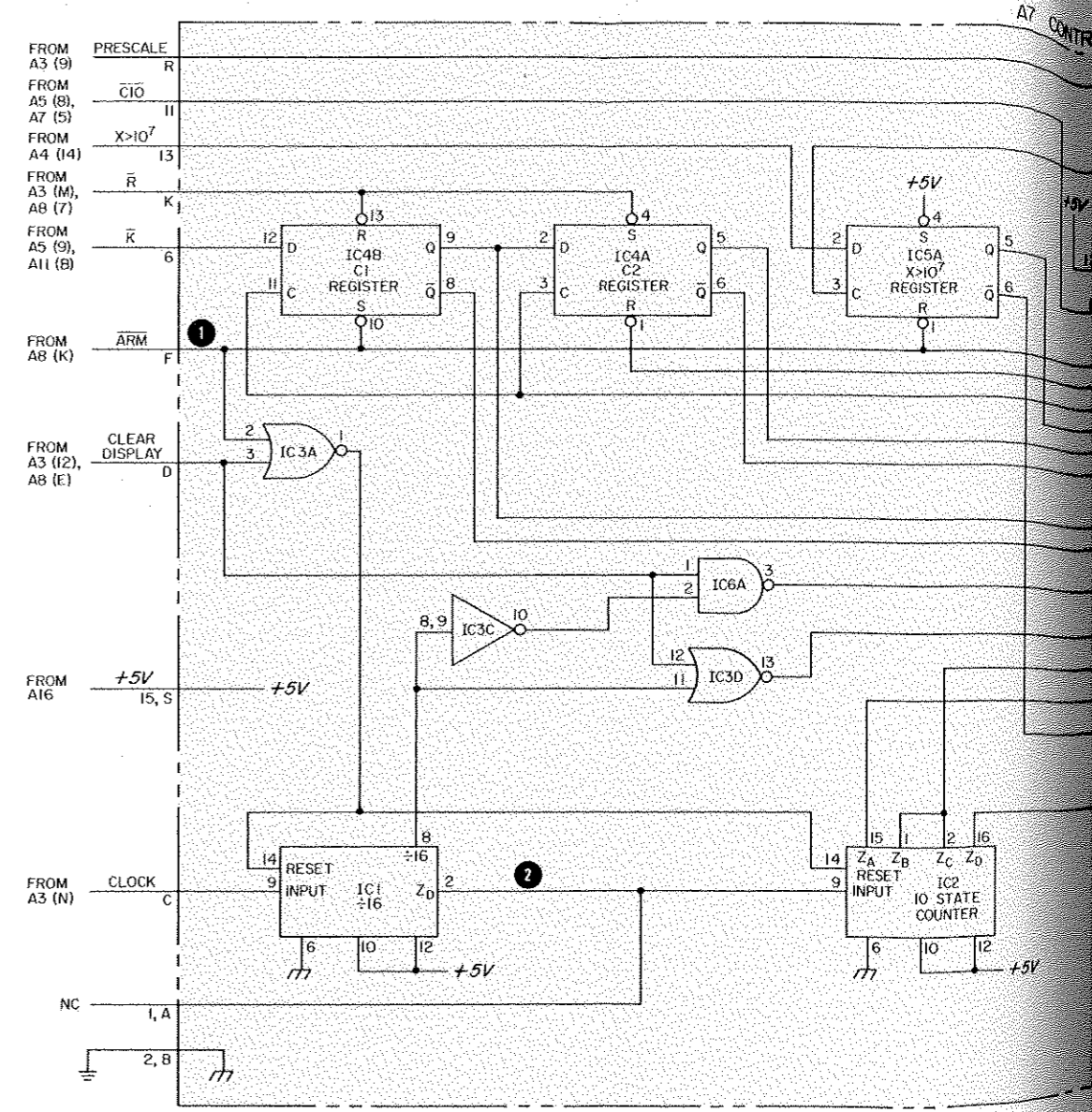
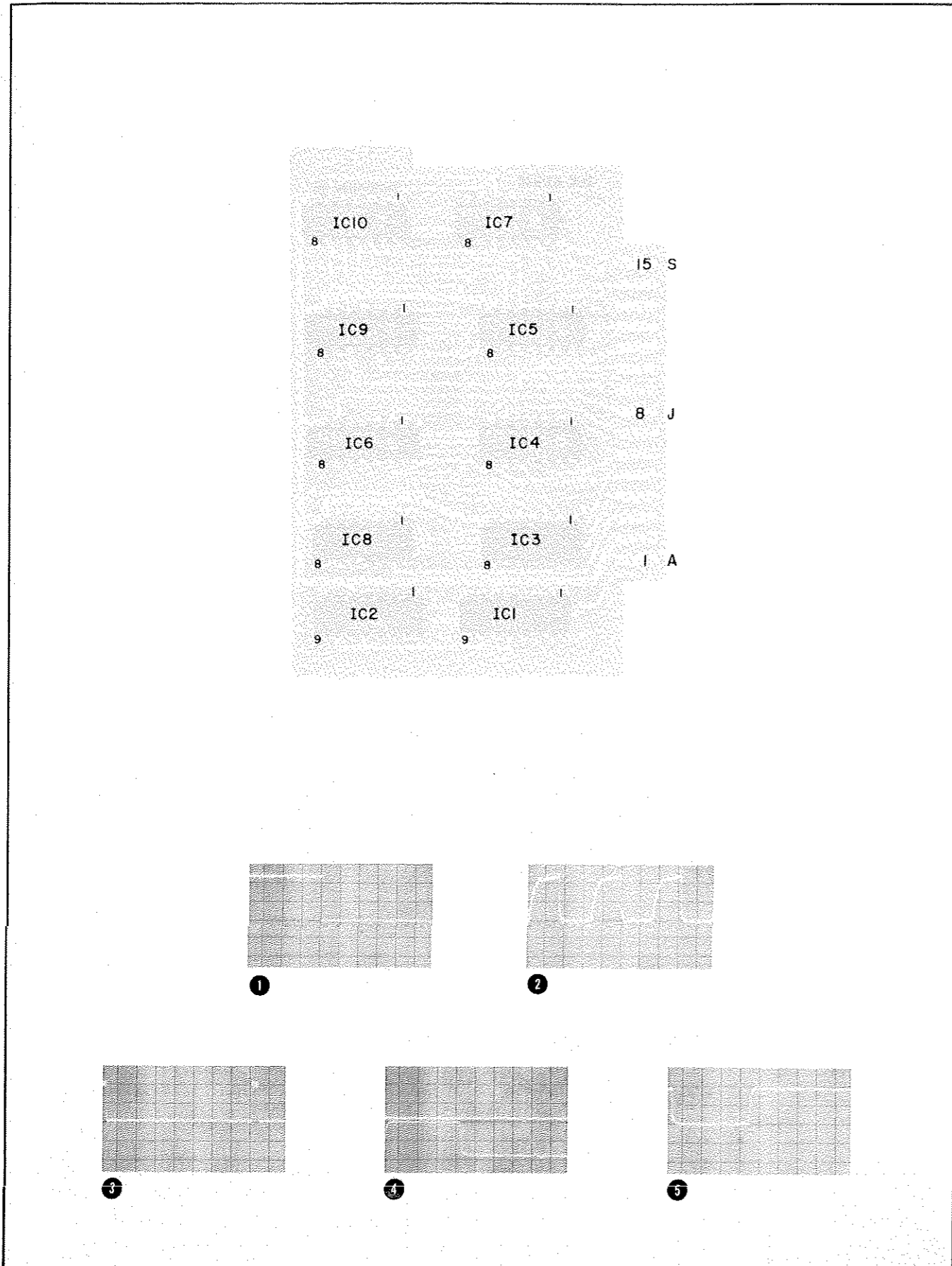
All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

WAVEFORM NO.	Oscilloscope Settings				
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM
1	.2		x	x	.1 ms
2	.2		x	x	.5 $\mu$ s
3	.2		x	x	2 $\mu$ s
4-Upper	.2(1)		x	x	50 $\mu$ s
4-Lower	.2(1)		x	x	.2 $\mu$ s
5	.2		x	x	.2 $\mu$ s

(1) Baseline of each trace corresponds to zero volts dc.

Table 8-3. A7 Output Signal States at End of Reset and Arming

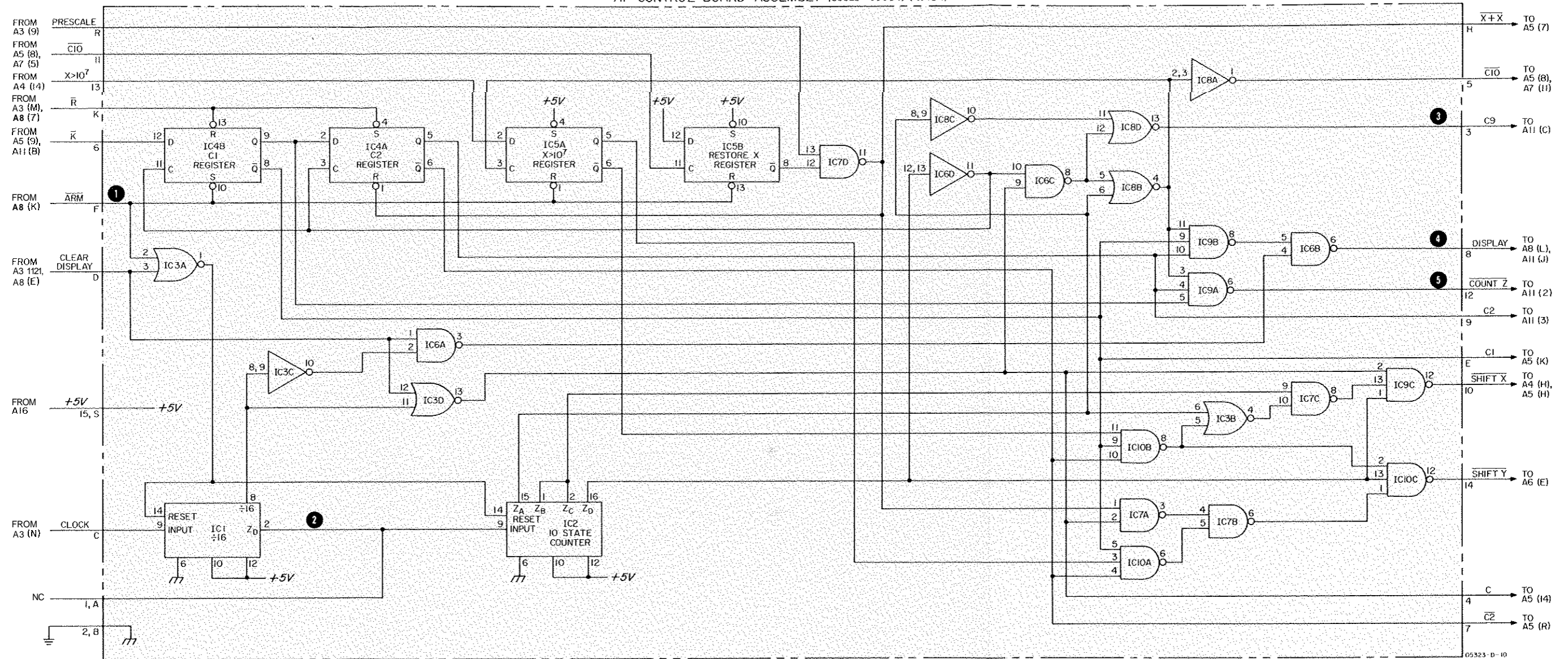
SIGNAL	A7 PIN	STATE (POSITIVE LOGIC)
$\bar{X} + \bar{X}$	H	LOW
$\bar{C}10$	5	HIGH
C9	3	
DISPLAY	8	
COUNT Z	12	HIGH
C2	9	
C1	E	
SHIFT X	10	HIGH
SHIFT Y	14	HIGH
C	4	LOW
$\bar{C}2$	7	HIGH



NOTES

1 REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED ADO ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION

A7 CONTROL BOARD ASSEMBLY (05323 - 60004) (NOTE 1)



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBER
IC1	1820-0209
2	1820-0119
3.8	1820-0328
4.5	1820-0077
6.7	1820-0054
9.10	1820-0068

REFERENCE DESIGNATIONS

A7
IC1-10

Figure 8-9. A7 Control Board Assy



A8 OPERATION

At the start of the Gate cycle, the  $\overline{\text{GATE}}$  signal will go LOW which resets the D-Register to D = 15 (outputs are LLLL). At the end of the Gate cycle, the GATE signal will go HIGH which resets the D-Register to D = 0 (outputs are HHHH). At D = 0 the MSD signal goes HIGH, which allows transfer of the MSD to the Display as soon as a DISPLAY pulse occurs. Each time a COUNT D pulse occurs, the D-Register will be advanced, and a new transfer pulse will occur. D = 7 is a blank state. At D = 8, the  $\overline{\text{R}}$  signal will go LOW, which resets all registers. Also, at D = 8, the  $\div 10$  output from the D-Register, IC1(8), will go LOW. The  $\overline{\text{PRINT}} = \text{LOW}$  signal enables a Digital Recorder, if used. At D = 9, the ARM signal will go LOW, which rearms the counter for the next Gate cycle.

When the BLANKING switch is ON and reset occurs, the first zero is displayed and the other Display positions are blanked. This process is accomplished by IC8D and the Blanking flip/flop (IC5A and IC9B) when the CLEAR DISPLAY signal goes HIGH at IC8D13. The Compute cycle starts, and the MSD is transferred to the Display at D = 0. When D = 1, the  $\overline{\text{T2}}$  signal goes LOW, and the IC8D12 input becomes HIGH. Output IC8D11 now goes LOW which makes  $\overline{\text{BLANK Z}}$  go LOW. Even though a transfer pulse was generated for the second Display digit, the blanking signal causes a blank-digit display. As the  $\overline{\text{T3}}$  through  $\overline{\text{T7}}$  transfer pulses are generated, blanking of the third through seventh Display digits will also occur.

Automatic blanking of the sixth and/or seventh Display digits will occur when Counter resolution limits are exceeded, if the BLANKING switch is ON. Gate IC9C controls the Blanking flip/flop for sixth digit transfer; gates IC8B and IC8C control the Blanking flip/flop for seventh digit transfer. Table 8-4 shows the gate input/output relationships and  $\overline{\text{BLANK Z}}$  level at T6 and T7. Operation of the Blanking flip/flop may be inhibited by setting S4 (BLANKING) to OFF, which makes  $\overline{\text{BLANK Z}}$  always HIGH. In this case, the Display may indicate false resolution in the sixth and seventh digits, if the selected measurement time is too short. Refer to Section III for resolution vs. measurement time considerations.

Table 8-4.  $\overline{\text{BLANK Z}}$  Level at D = 5 and D = 6

MEASUREMENT TIME	S7 = Hz				S7 = RPM			
	MSD < 2 = HIGH	MSD < 2 = LOW	MSD < 2 = HIGH	MSD < 2 = LOW	MSD < 2 = HIGH	MSD < 2 = LOW	MSD < 2 = HIGH	MSD < 2 = LOW
.2 = LOW	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LOW
.1 = LOW	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LOW
.04 = LOW	HIGH	LOW	LOW	LOW	HIGH	LOW	HIGH	LOW
.01 = LOW	HIGH	LOW	LOW	LOW	HIGH	LOW	HIGH	LOW
	D = 5	D = 6	D = 5	D = 6	D = 5	D = 6	D = 5	D = 6

A8 TROUBLESHOOTING

Check the +5 Vdc at pin 15, S. Check the  $\overline{\text{GATE}}$ , COUNT D and DISPLAY waveforms. Examine the Za, Zb, Zc, Zd outputs from the D Register; the Za waveform should show D = 0 through D = 9 (or D = 15) levels. Check the MSD,  $\overline{\text{T2}}$ ,  $\overline{\text{T3}}$ ,  $\overline{\text{T4}}$ ,  $\overline{\text{T5}}$ ,  $\overline{\text{T6}}$  and  $\overline{\text{T7}}$  transfer pulse waveforms; all pulses should be similar, except for  $\overline{\text{T4}}$  which is a long pulse (approximately 50  $\mu\text{sec}$ ). If any transfer pulses are missing, check the gates between the D-Register and the signal output with the Logic Probe. Check the  $\overline{\text{R}}$ ,  $\overline{\text{ARM}}$ , and ARM waveforms with an oscilloscope. If any of these signals are missing, use the Logic Probe to isolate the defective gate element.

If the blanking feature does not operate in accordance with Table 8-4, check the levels of the RPM, MSD < 2, .2, .1, .04, .01, and BLANKING signals with the Logic Probe while operating the Hz/RPM, MEASUREMENT TIME, and BLANKING switches.  $\overline{\text{BLANK Z}}$  can be checked with the oscilloscope, and the Logic Probe can be used to isolate a defective gate element in the Blanking Logic or a defective Blanking flip/flop.

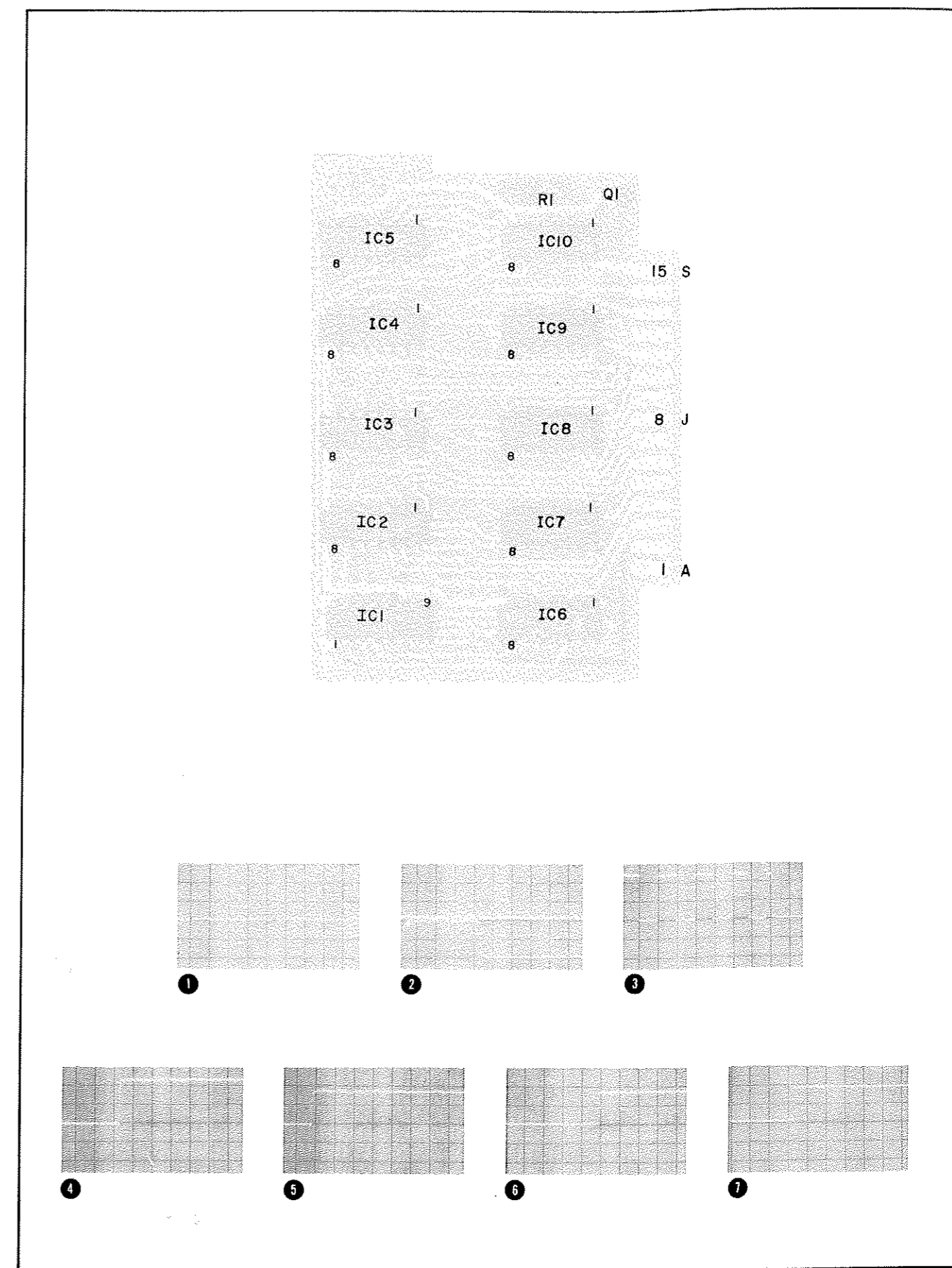
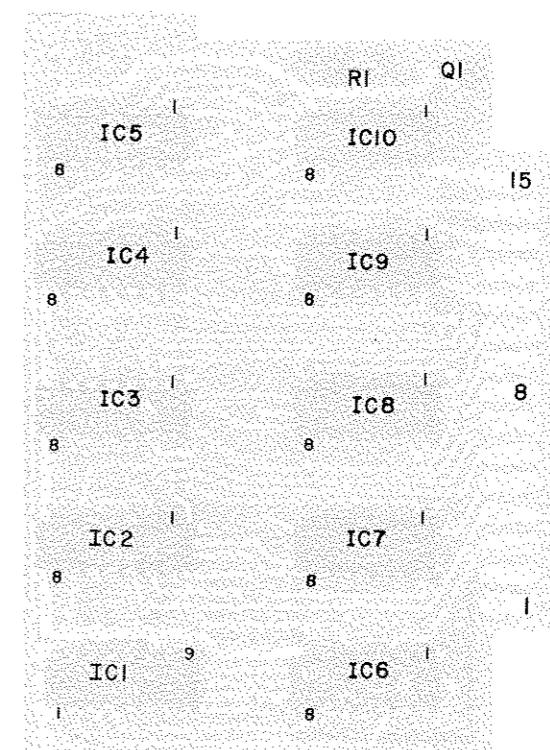
COUNTER SETTINGS

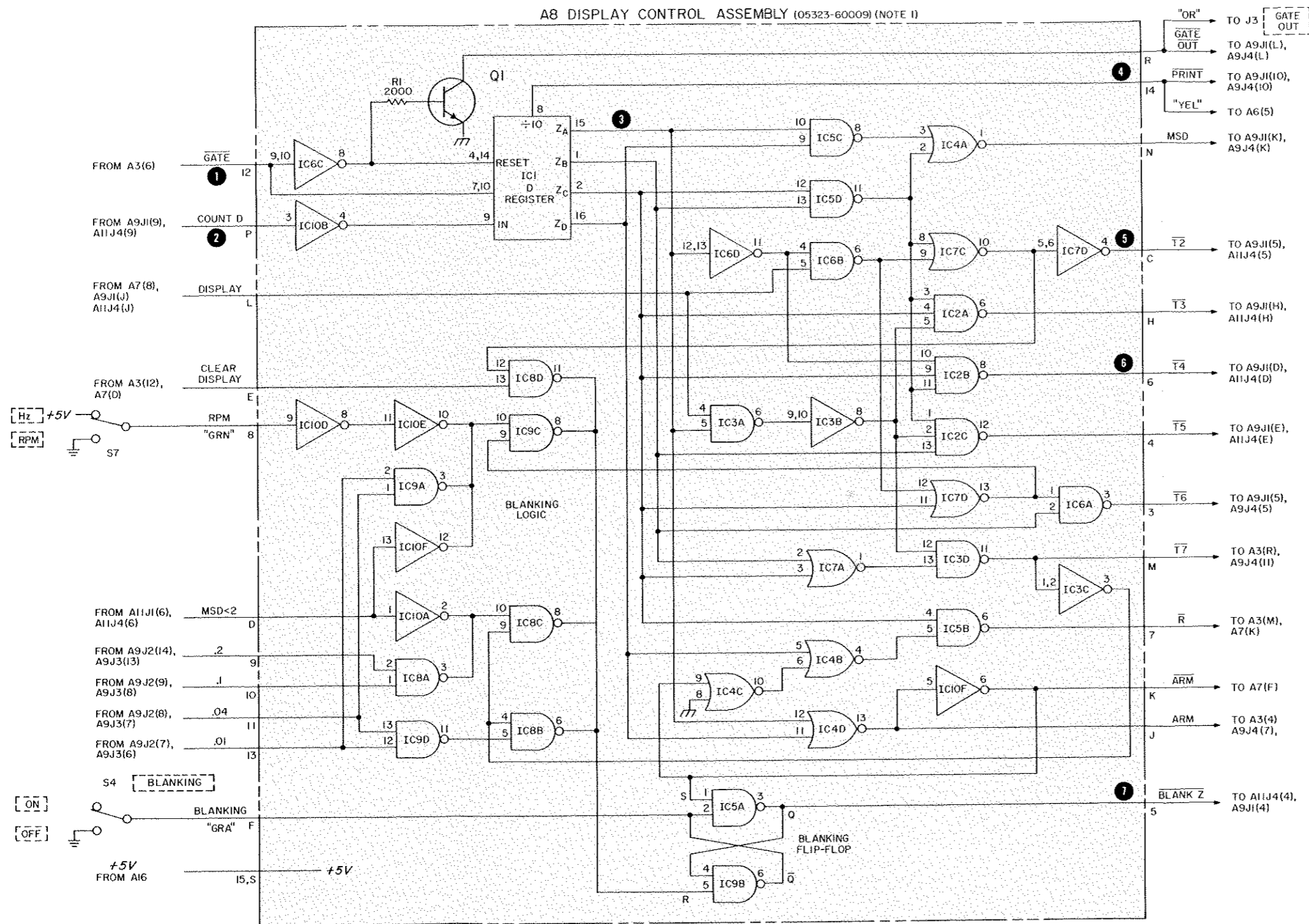
MODE . . . . . CHECK  
MEASUREMENT TIME . . . . . .01  
TIME BASE . . . . . INT  
Hz/RPM . . . . . Hz  
BLANKING . . . . . ON

All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

WAVEFORM NO.	Oscilloscope Settings				
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM
1	.2		x	x	2 ms
2-Upper	.2(1)		x	x	50 $\mu\text{s}$
2-Lower	.2(1)		x	x	.2 $\mu\text{s}$
3	.2		x	x	50 $\mu\text{s}$
4	.2		x	x	5 $\mu\text{s}$
5	.2		x	x	.5 $\mu\text{s}$
6	.2		x	x	10 $\mu\text{s}$
7	.2		x	x	20 $\mu\text{s}$

(1) Baseline of each trace corresponds to zero volts dc.





**NOTES**

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY NUMBER ARE ABBREVIATED FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC1	1820-0119
2	1820-0068
3,5,6	1820-0054
4,7	1820-0328
8,9	1820-0094
10	1820-0307
Q1	1854-0071

REFERENCE DESIGNATIONS

NO PREFIX	A8
	IC1-10
	Q1
S4,7	R1

05323-0-11

Figure 8-10. A8 Display Control Board Assy 8-19

AS OPERATION

COUNTER SETTINGS

The A9 Connector Board Assembly serves as an interface and test board for the Counter. Interboard connections are made between connectors XA2-XA8 and XA17 ( $\pm 12V$  Supply). Connector J1 is a test connector with critical signals available at its pins. Connector J2 is connected by a wiring harness directly to J6, REMOTE PROGRAM connector. Connector J3, push-on connectors, and hard-wiring are used to connect to other points within the Counter. Connector J4 is a pressure connection to A11.

AC POWER. . . . . OFF-ON-OFF  
MODE . . . . . CHECK  
MEASUREMENT TIME. . . . . .04  
TIME BASE . . . . . INT

All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time base plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

L1 through L8 are decoupling chokes. C1, R1, and CR1 are used to supply a reset pulse to A3 when the Counter is turned on.

WAVEFORM NO.	Oscilloscope Settings				
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM
1	.2		x	x	.2 sec

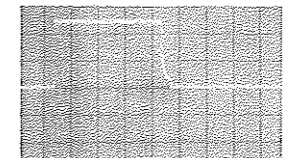
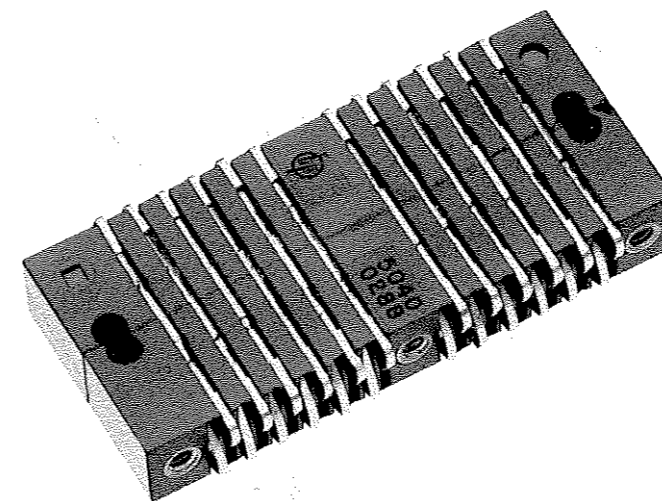
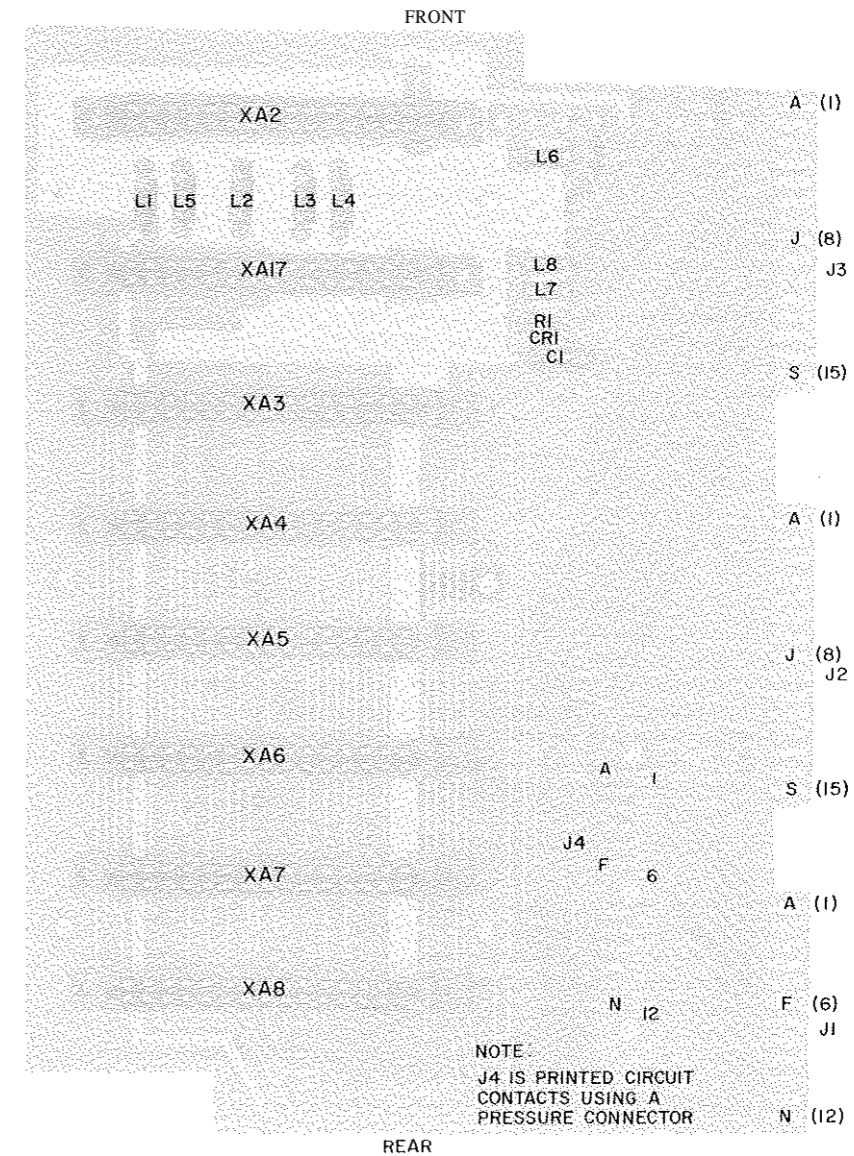
Table 8-5. Open Choke Symptoms

OPEN CHOKE	POWER ABSENT	
	VOLTAGE	LOCATION
L1	+5	
L2	+12	A2(8, J)
L3	+12	A2(7, H)
L4	-12	A2(6, F)
L5	-12	A2(P)
L6	LEVEL	A2(3, C)
L7	+12	A15(WHT-VIO) and TP(1)
L8	-12	A15(VIO)

(1) +12V Test Point (TP) located between A15 and J7.

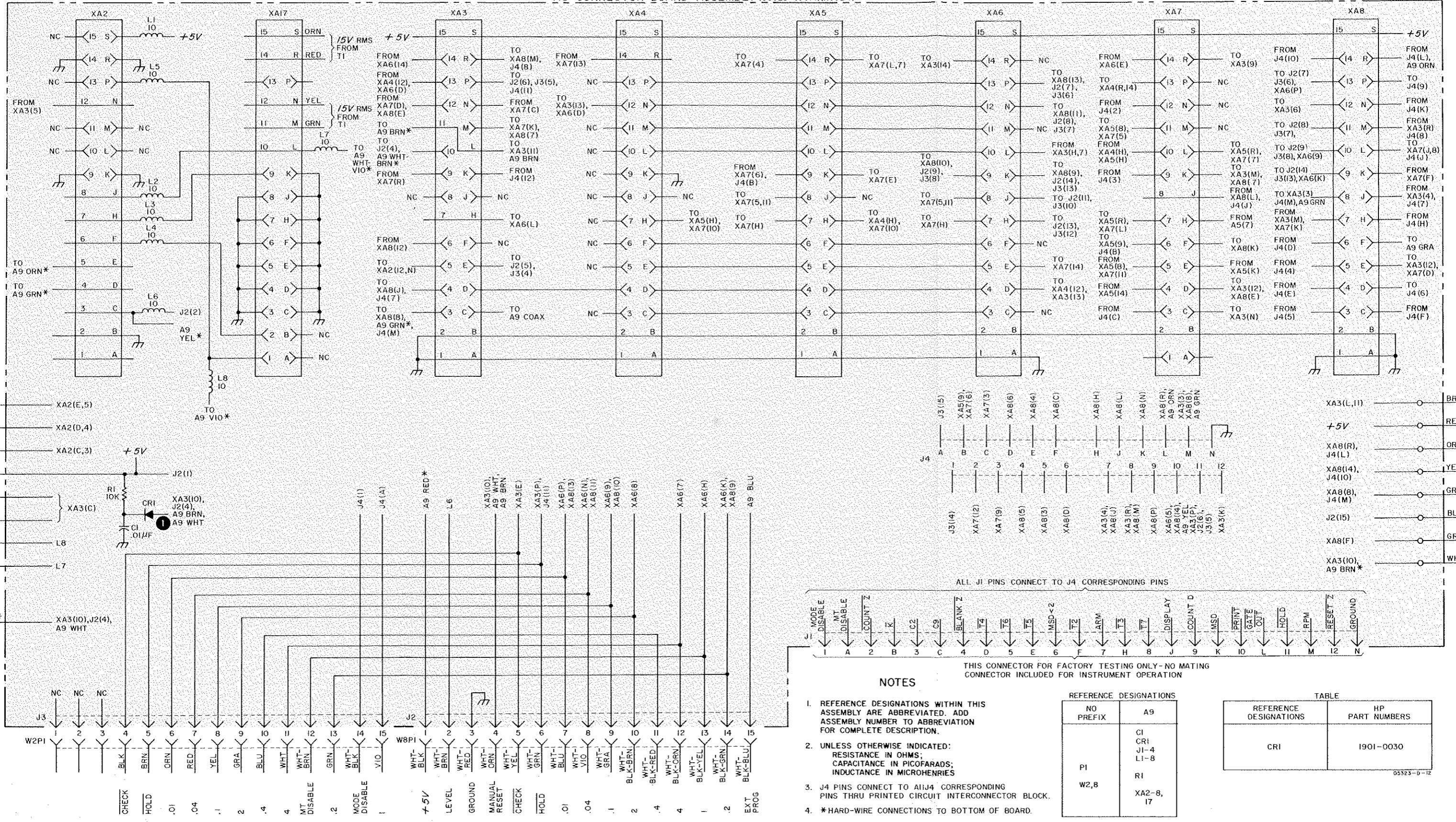
A9 TROUBLESHOOTING

Troubles in A9 can be determined by checking waveforms or logic levels at the inputs and outputs of the Counter PC boards. When power or a signal is absent at its normal destination, the Logic Probe, DC Voltmeter, or Oscilloscope can be used to locate the fault. If any of the chokes (L1-L8) are open, voltage will be absent as shown in Table 8-5. The oscilloscope can be used to check for excessive ripple or noise, which would indicate a shorted choke. Check the MANUAL RESET line waveform if the Counter fails to reset when ac power is applied.



0

A9 CONNECTOR BOARD ASSEMBLY (05323-60014)(NOTE 1)



**NOTES**

- REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
- UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS; CAPACITANCE IN PICO FARADS; INDUCTANCE IN MICROHENRIES
- J4 PINS CONNECT TO A11J4 CORRESPONDING PINS THRU PRINTED CIRCUIT INTERCONNECTOR BLOCK.
- \*HARD-WIRE CONNECTIONS TO BOTTOM OF BOARD.

Figure 8-11. A9 Connector Board Assy

## A10 OPERATION

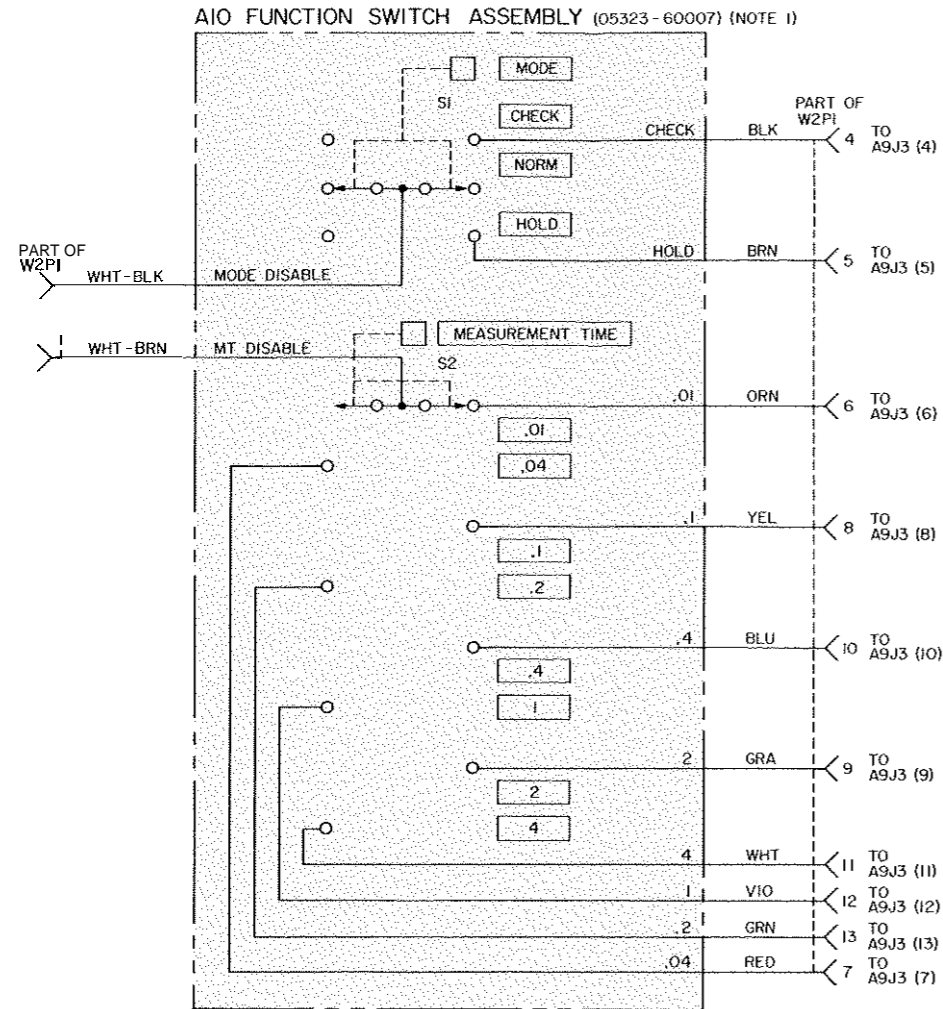
When the EXT PROG signal from J6, REMOTE PROGRAM connector is HIGH (no connection) the MODE DISABLE and MT DISABLE signals from A11 will be LOW. This makes the wipers of the MODE switch (S1) and MEASUREMENT TIME switch (S2) LOW. As the switch position is varied, a LOW will appear at the selected contact. When the EXT PROG signal is LOW, S1 and S2 will be disabled, allowing their functions to be remotely programmed through J6, REMOTE PROGRAM connector.

## A10 TROUBLESHOOTING

Use the Logic Probe to verify that the MODE DISABLE and MT DISABLE signals are both LOW with no connection to J6(15), EXT PROG. Ground EXT PROG, J6(15), and check to see that both signals are now HIGH. If the above tests fail, trace the signals through A9 and A11 to J6 with the Logic Probe. Check the switch outputs with the Logic Probe while operating S1 and S2. Make sure that only one output from S1 and one output from S2 are LOW at any time, when J6 is not in use (additional LOW levels indicate shorted gates or wiring).

S1

S2

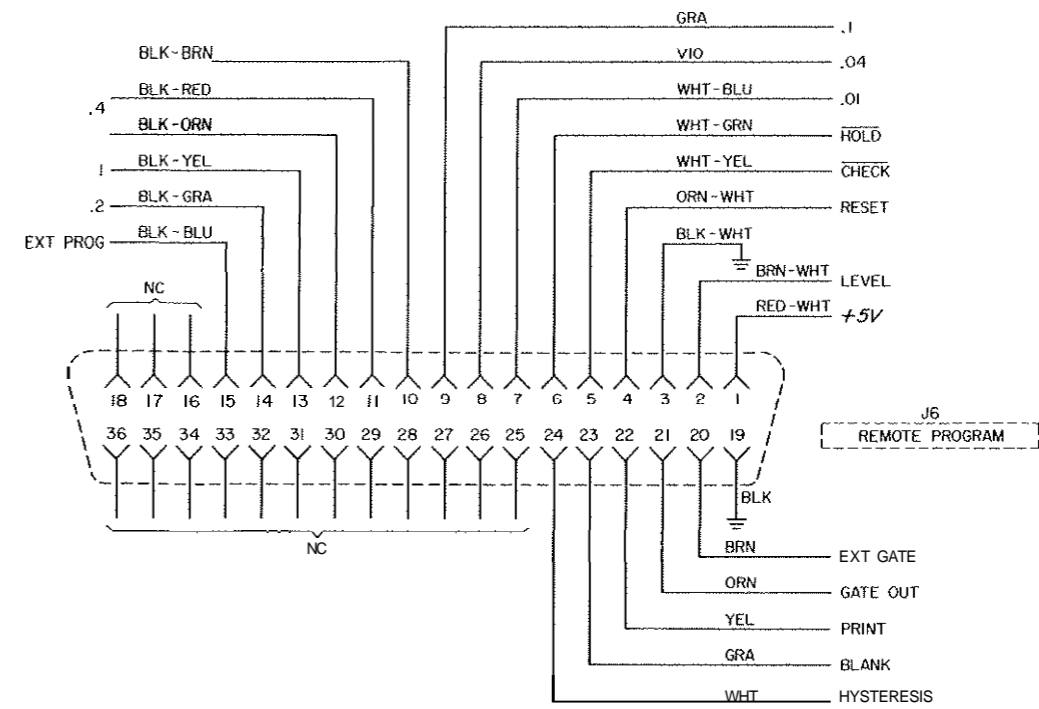
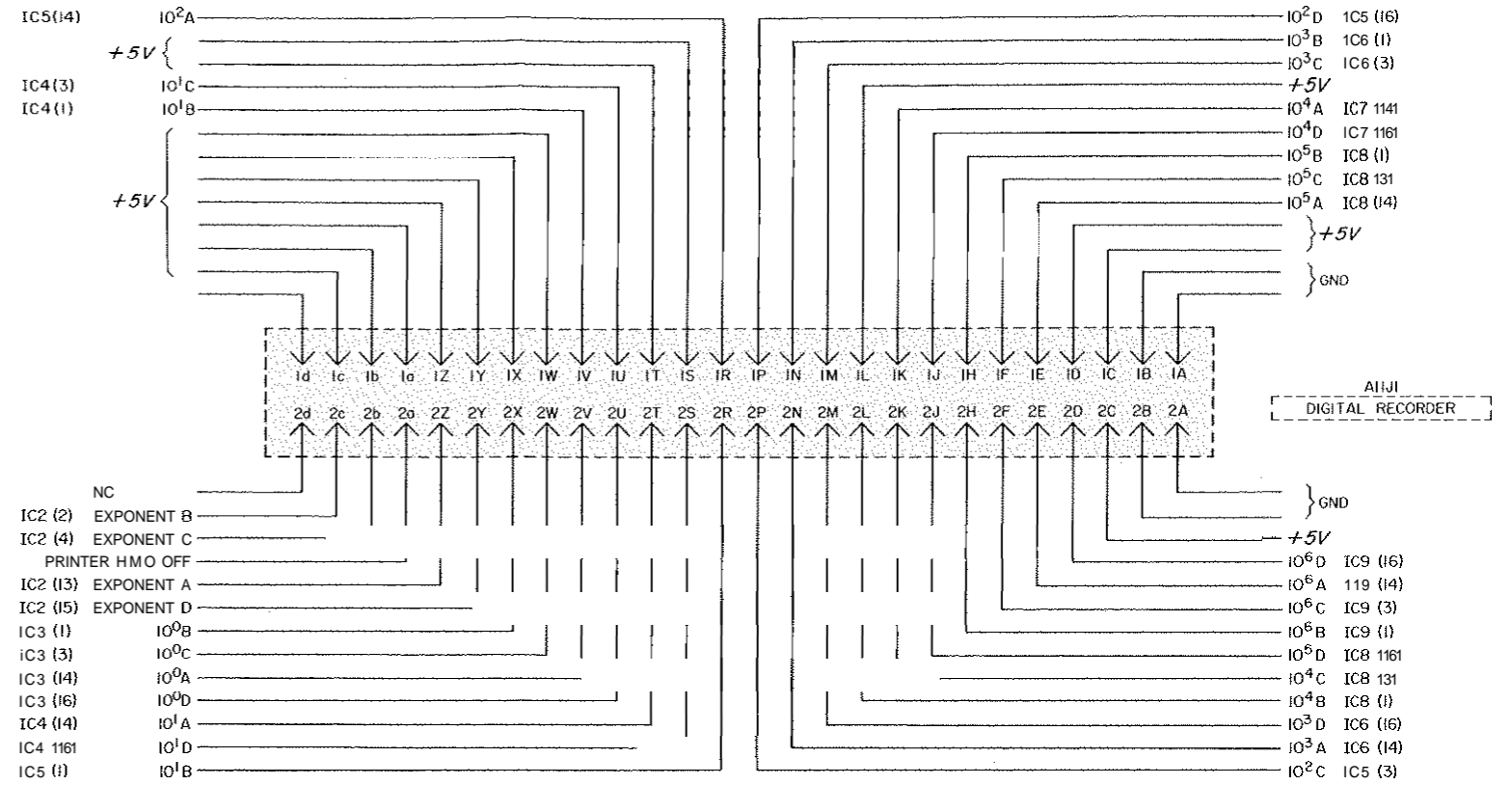


**NOTES**

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION

**REFERENCE DESIGNATIONS**

NO PREFIX	AIO
P1	S1,2
W2	



05323 0 3

Figure 8-12. A10 Function Switch Board Assembly  
J6, Remote Program Connector  
A11J1, Digital Recorder Connector

## A11 OPERATION

Each time the  $Xc + Y$  and  $X + Y$  operations are performed during the Compute cycle, either a DISPLAY or  $\overline{\text{COUNT Z}}$  pulse will be produced by A7. DISPLAY will be HIGH if a carry occurs, and  $\overline{\text{COUNT Z}}$  will be LOW each time a carry does not occur. The initial DISPLAY pulses determine the decimal point location (exponent) and measurement unit that are displayed. If the first  $Xc + Y$  operation produces a carry pulse ( $\overline{K} = \text{LOW}$ ) a DISPLAY pulse will appear at IC16B10. No  $\overline{\text{COUNT Z}}$  pulse was generated, so the Q output of the Range Detector is still HIGH, and IC16B9 will be HIGH. The IC16B8 output and the Down input to the E-Register will also become LOW. The preset inputs to the E-Register determine the initial state of the register count. If the Hz/RPM switch, S7, is set to Hz, Ia, Ib, and Ic will be LOW, and Id will be HIGH. This will set the initial count to  $E = 7$ . If S7 is set to RPM, Ia, Ib, and Ic will be HIGH, and Id will be LOW. This will set the initial count to  $E = 8$ , which corresponds to a X10 operation (the clock frequency was also divided by 6, which results in a X60 operation for RPM).

The first DISPLAY pulse causes the E-Register to change to  $E = 6$ . The second DISPLAY pulse would make  $E = 5$ , etc., until a  $\overline{K} = \text{LOW}$  signal fails to occur. Therefore, the E-Register stores the number of times that a carry pulse was generated until a  $\overline{\text{COUNT Z}}$  pulse occurs (successful subtraction). Each time an initial carry pulse occurs during the  $Xc + Y$  operation, the X-Register contents are multiplied by 10, and  $Xc + Y$  is tried again. The E-Register is actually counting the number of times that the X10 operation occurs before a successful subtraction ( $X + Y$ ) occurs. Notice that no COUNT D pulses are generated even though DISPLAY pulses are occurring, because IC16D13 is LOW at this time.

When the first  $\overline{\text{COUNT Z}}$  pulse occurs the Range Detector will be reset to  $Q = L$ ,  $\overline{Q} = H$ . The  $Q = \text{LOW}$  appears at IC16B9 to disable the Down input to the E-Register. The Z-Register (IC18) will advance to  $Z = 1$ . Each time a  $\overline{\text{COUNT Z}}$  pulse occurs, Z will advance by one count. When a carry finally occurs, a DISPLAY pulse will be produced at IC16A5 and IC16D12. The HIGH input to IC16D12 will cause a COUNT D pulse to occur, and the two HIGH inputs to IC16A produce a LOW G2 input to IC9(5) which transfers the contents of the Z-Register to the Buffer Storage Register, IC8, and A12. The MSD has now been transferred to the Display, and the computer restores the remainder and performs a X10 operation. This sequence is repeated for the 2nd, 3rd, and 4th digits. When  $\overline{T5} = \text{LOW}$ , the fifth digit is transferred to the Display, and the G1 input to the E-Buffer Storage Register goes LOW. The 4-bit BCD exponent information will now be transferred from IC12 (15, 16, 1, 2) to IC14 (14, 1, 3, 16). The IC14 outputs appear as inputs to the Exponent/Measurement Unit Decode Logic, consisting of part of IC1, IC2, IC10, and IC11 and transistors Q1, Q2, and Q3. The Decode Logic outputs are as shown in Table 8-6. The J2 outputs

control the decimal point location via A12. For  $E = 5$ , 4, or 3, the J2 outputs are different as a function of the S7 position; this difference is caused by the  $\pm 60$  operation, which can shift the decimal point position. Notice that when  $E = 0$ , all inputs to IC15B will be HIGH, and a LOW will appear at IC15B8 and IC19C9, which resets the Range Detector to  $Q = L$ ,  $\overline{Q} = H$ . This inhibits IC16B, disabling the E-Register and allowing the remaining digits to be displayed even if they are zeros.

At  $\overline{T6} = \text{LOW}$ , the sixth digit will be transferred from the Z-Register via IC4 to A12. At  $\overline{T7} = \text{LOW}$ , the seventh digit will be transferred, and a HIGH will appear at IC12(6), the preset input, which presets the E-Register to  $E = 8$  or  $E = 7$ .

The Z-Register is reset to  $Z = 0$  after each digit has been calculated. The reset is accomplished by gates IC21A and IC22D. When a carry occurs during the compute cycle, the remainder is restored, and a X10 operation is initiated by  $C2 = \text{LOW}$ . This  $CZ = \text{LOW}$  signal appears at IC19D12, causing IC19D11 to go HIGH. The blanking conditions have been previously described as part of A8. When a  $\overline{\text{BLANK Z}}$  = LOW signal occurs, one input to gates IC13(A, 3, C, D) will go LOW. This presents a blank state (binary 15) to the Buffer Storage Registers (IC3-IC9).

If the HYSTERESIS switch, S5, is OFF, input IC21B10 will be LOW, which makes IC21B8 always HIGH. Gate IC16C will be enabled, allowing gating of COUNT D pulses, and the Up input to the E-Register will be disabled. By setting S5 to ON, input IC21B10 will be HIGH. When the other inputs to IC21B are HIGH, IC21B8 will go LOW. Input IC21B9 will be HIGH when  $Z = 8$  or 9,  $\overline{K} = \text{HIGH}$  (no carry pulse), and  $C9 = \text{HIGH}$ . IC21B12 will be HIGH if  $\text{MSD} = \text{HIGH}$ . IC21B13 will be HIGH if the  $\overline{Q}$  output of the  $\text{MSD} < 2$  Memory is HIGH, which occurs only when  $Z = 1$  or Blank ( $\text{MSD} < 2$ ). Suppose that the MSD changes from 1 to 9 (which might cause the Display and measurement unit to change if hysteresis was not used). Before the  $\text{MSD} < 2$  Memory can change state, its  $\overline{Q}$  output will be HIGH. A LOW output at IC21B8 will occur which produces an extra COUNT D pulse (setting  $D = 1$  in the Display Register) and an Up input pulse to the E-Register. The first digit of the Display will remain blanked. The first digit of F (9) will be loaded at  $\overline{T2} = \text{LOW}$  into the second Display position. The change in exponent shifts the decimal point to maintain the correct measurement unit and decimal point.

The  $\overline{\text{HOLD}}$  signal will be HIGH until Q5 conducts, which causes  $\overline{\text{HOLD}} = \text{LOW}$ . Q5 will conduct when J1-2(a) goes HIGH, which prevents the Display from changing while the Digital Recorder is printing the data (HOLD-OFF VOLTAGE).

The  $\overline{\text{PRINT}}$  signal will go LOW when  $D = 8$ . It is available at J1-1(d) for a Digital Recorder (PRINT COMMAND). Two gates (IC11C and IC11A) are used as inverters for the EXT PROG signal to supply the MODE DISABLE and MT DISABLE signals to A10.

## A11 TROUBLESHOOTING

Check the +5 Vdc at the red push-on connector. Use the oscilloscope to check transfer, DISPLAY,  $\overline{\text{COUNT Z}}$ ,  $\overline{K}$ , C9, ARM, COUNT D and RESET Z waveforms. If the exponent or measurement unit displayed is incorrect, use the Logic Probe with Table 8-6 to check the E-Register, E-Buffer Storage Register, signal  $\overline{\text{RPM}}$  and the Decimal/Measurement Unit Decode Logic. Observe the waveforms of the Za output of the E-Register and reset input of the Range Detector.

To check the operation of the Z-Register and Buffer Storage Registers, connect a clip lead between the bare test point (located between IC15 and IC19, top of A11 board) and chassis ground. With the MEASUREMENT TIME set to 1, the Display should shift from 11.1111 MHz through 88.8888 MHz to 99.9999 MHz as long as the test point is grounded. Use the Logic Probe to isolate a defective Buffer Storage Register. The oscilloscope may be used to monitor the input and gate waveforms for the Buffer Storage Register.

Incorrectly displayed digits may be caused by failure of the Z-Register to reset correctly. Observe the waveforms at the reset (test point may be used) and input pins of the Z-Register with the oscilloscope. Blanking operation may be checked by observing the  $\overline{\text{BLANK Z}}$  waveform and operation of the four blanking gates (IC13A-D). Check the operation of the hysteresis circuits by decreasing the input frequency so that the MSD changes from 1 to 9 and observe the waveforms at IC21B8 and IC12(15); also, check the  $\text{MSD} < 2$  signal with the Logic Probe. The  $\text{MSD} < 2$  Decode Logic may be checked with the oscilloscope or Logic Probe (test point grounded). If the  $\overline{\text{ARMED}}$  or COUNTING signals do not occur, check the waveform of the GATE OUT signal (J3) and IC1B8. Operation of Q4, Q5, IC11A and IC11C may be checked with the Logic Probe. An erratic GATE OUT signal may be caused by an open COUNTING lamp.

If COUNT D pulses are not generated correctly and the trouble is difficult to isolate, a dual-trace oscilloscope is helpful. Both inputs to a dual NAND or NOR gate may be monitored with the A and B inputs while the oscilloscope is externally triggered by the DISPLAY signal. This technique is also useful when troubleshooting a problem in the hysteresis circuits ( $\text{MSD} < 2$  Decode Logic,  $\text{MSD} < 2$  Memory, Hysteresis Gate) or display circuits (Z-Register, Range Detector, IC19D).

Fig  
A10 FUNCTION SWITCH BOARD  
J6, REMOTE PROGRAM CONN  
A11J1, DIGITAL RECORDER CONN

(See P:

COUNTER SETTINGS

A. MODE . . . . . NORM  
MEASUREMENTTIME . . . . . .01  
TIME BASE . . . . . INT  
LEVEL . . . . . PRESET  
ATTEN. . . . . X1  
AC-DC. . . . . DC  
Hz/RPM . . . . . Hz  
BLANKING . . . . . ON  
HYSTERESIS. . . . . ON  
INPUT . . . . . 10.2240 kHz, decrease  
to 9.9200 kHz

B. same as A, except:  
HYSTERESIS. . . . . OFF  
(Display should be 9.9200 kHz)

C. Same as A, except:  
INPUT . . . . . 10.2240 kHz

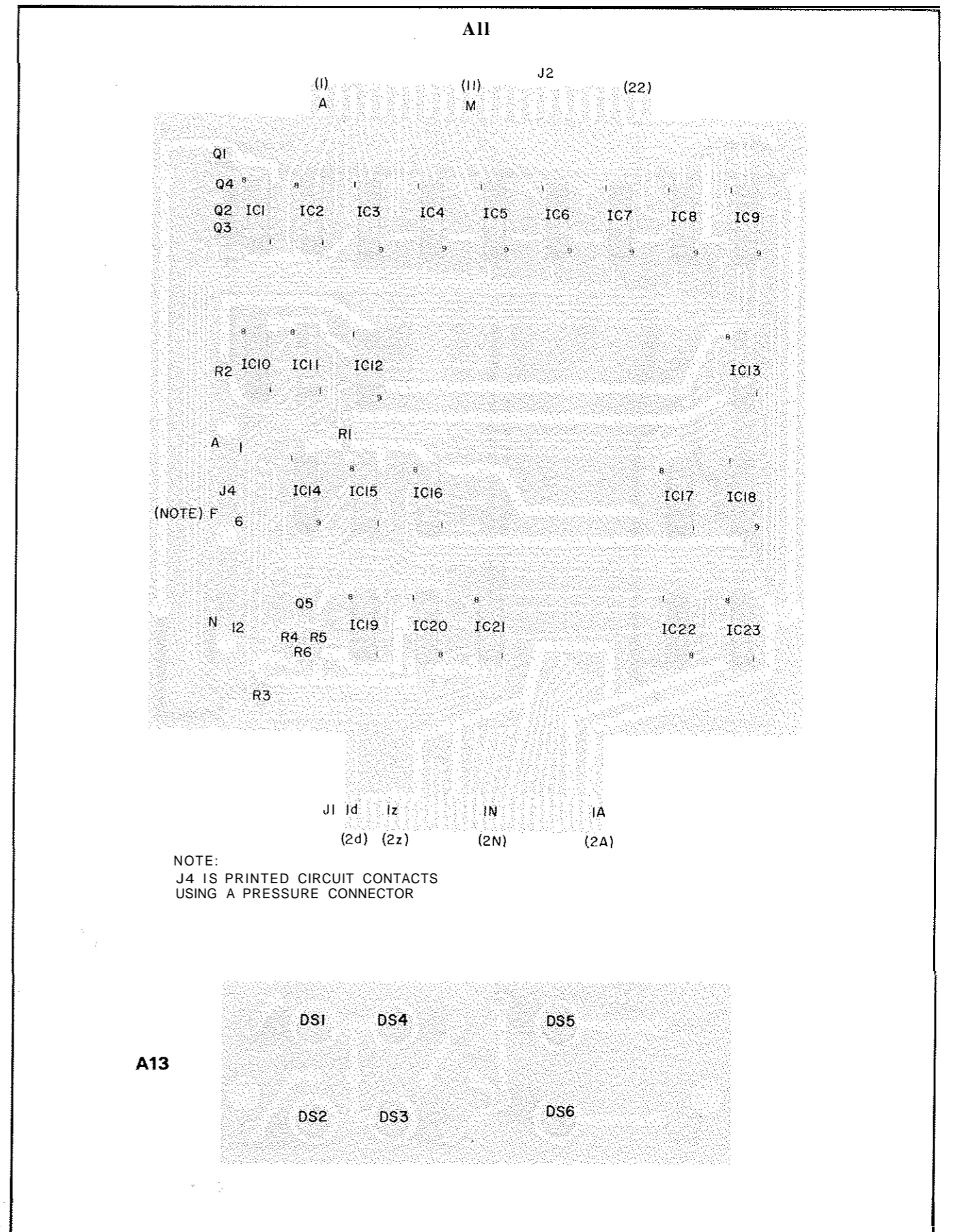
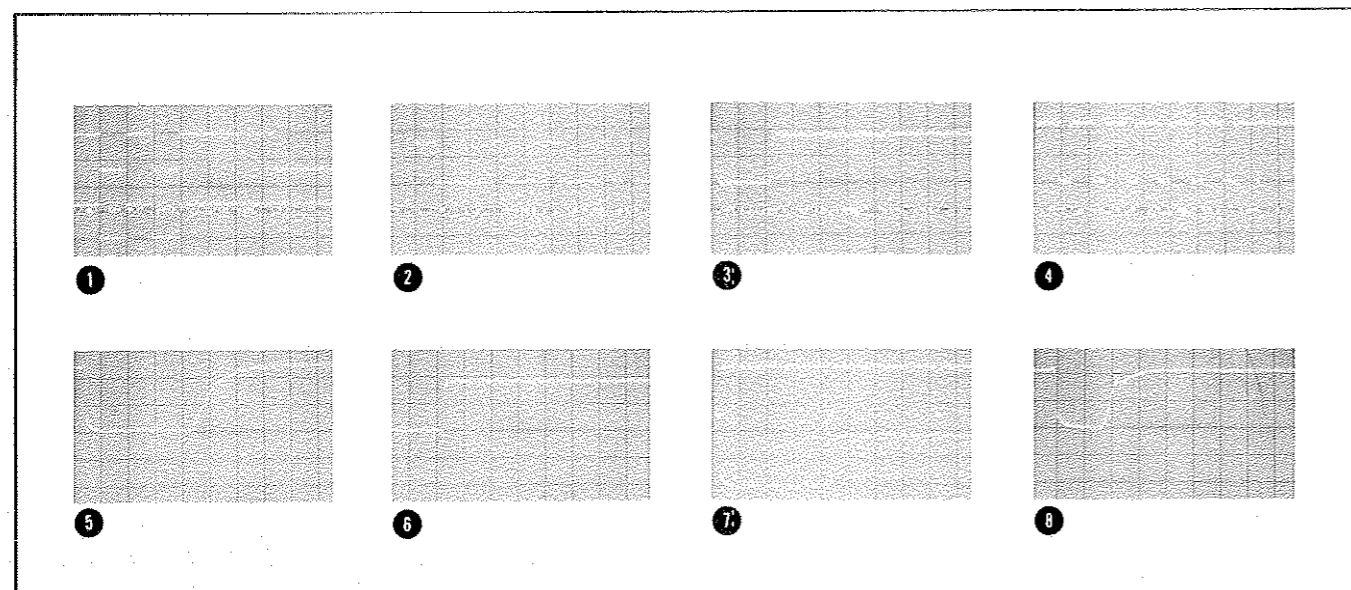
D. MODE . . . . . CHECK  
MEASUREMENTTIME . . . . . .01  
TIME BASE . . . . . INT

(Display should be X9.9200 kHz, where X = Blank digit.)

All waveforms taken with HP 180A Oscilloscope, HP 1801A Vertical Plug-in, HP 1821A Time Base Plug-in, HP 10004A 10:1 Divider Probe. Center line of graticule is zero volts.

WAVEFORM NO.	COUNTER SETTING	Oscilloscope Setting				
		SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM
1-Upper	A	.2(1)		X	X	50 $\mu$ s
1-Lower	B	.2(1)		X	X	50 $\mu$ s
2	C	.2		X	X	40 $\mu$ s
3	D	.2		X	X	.4 $\mu$ s
4	D	.2		X	X	40 $\mu$ s
5	D	.2		X	X	.2 $\mu$ s
6	A	.2		X	X	4 $\mu$ s
1-Upper	A	.2(1)		X	X	4 $\mu$ s
7-Lower	A	.2(1)		X	X	.2 $\mu$ s
8	D	.2		X	X	1 $\mu$ s

(1) Lower edge of traces corresponds to zero volts dc.





PART OF A11 MAIN BOARD ASSEMBLY (05323-60001) (NOTE 1)

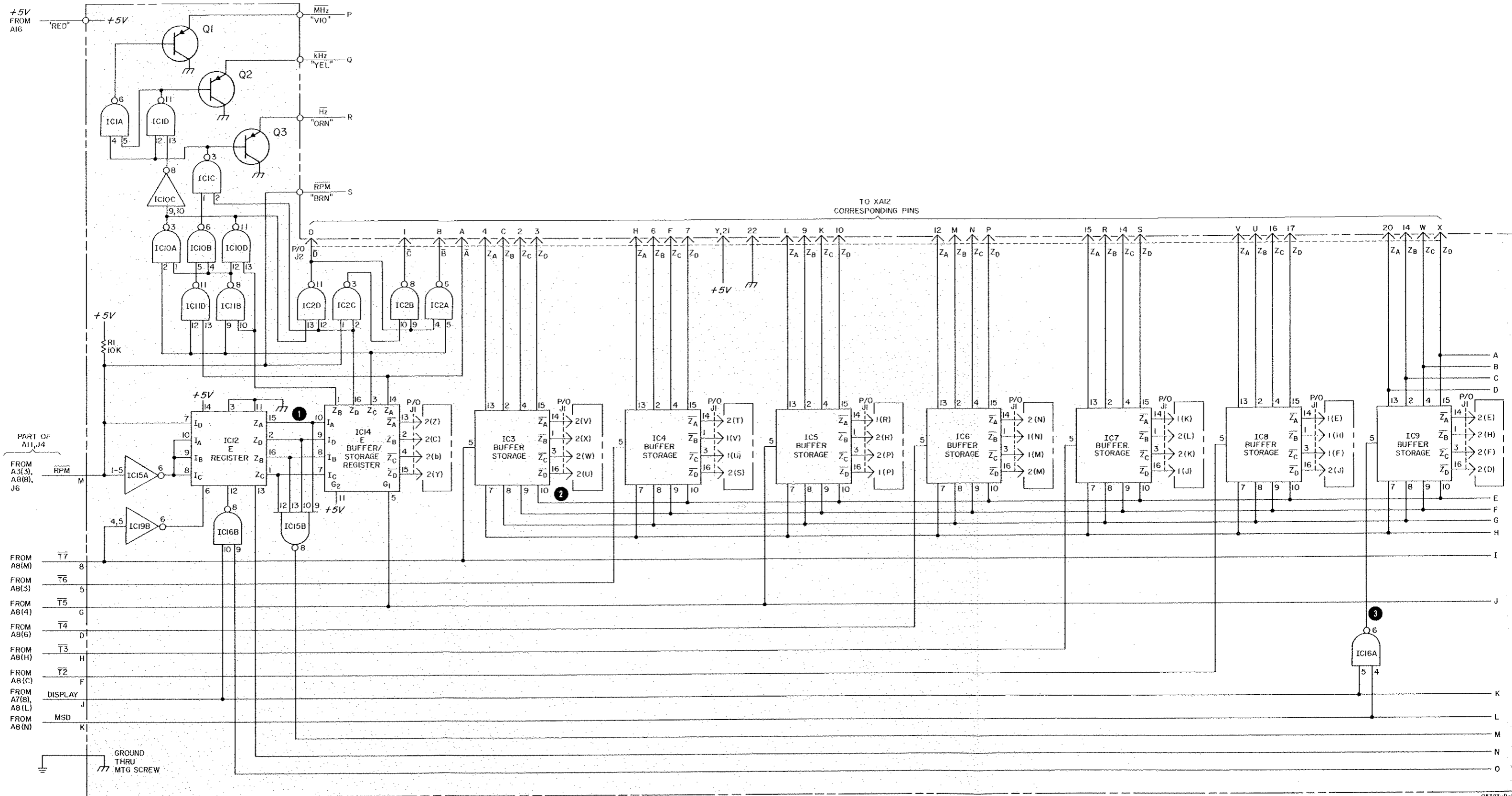


Figure 8-13. A11 Main Board Assy  
A13 Annunciator Board Assy  
(Sheet 1 of 2)

A13 OPERATION

The COUNTING, ARMED and RPM lamps receive +5 Vdc from A11 on the Red wire. COUNTING, ARMED and RPM will go LOW when enabled by A11 to complete the circuit and turn the lamp on. When the Hz/RPM switch (S7) is set to Hz, signal RPM will be HIGH, so the BRN wire will be at +5 Vdc. When the Exponent/Measurement Unit Decode Logic is enabled

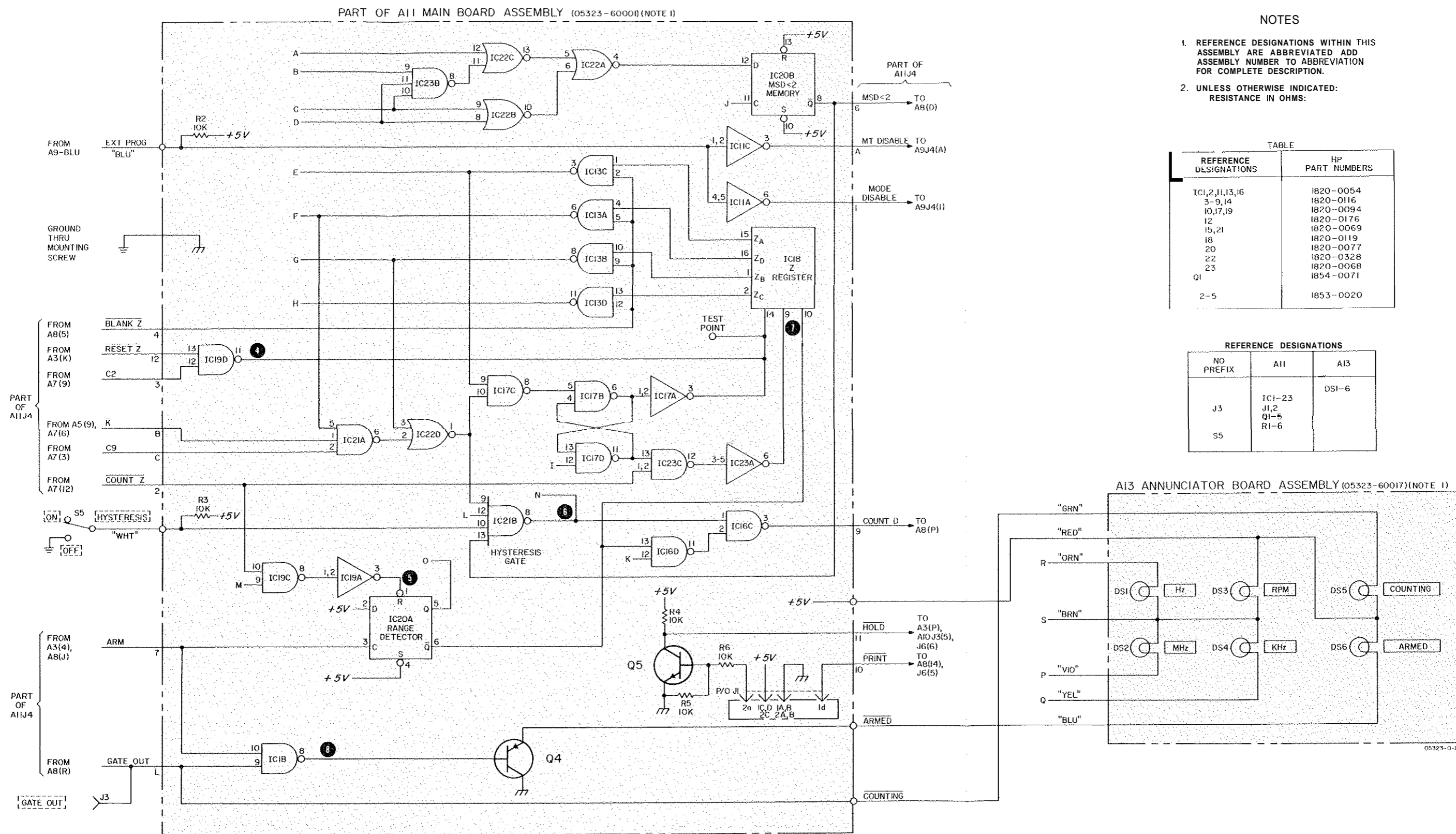
in A11 either the VIO, YEL, or ORN wires will go LOW to turn either the MHz, kHz, or Hz lamp on.

A13 TROUBLESHOOTING

Use the Logic Probe or DC Voltmeter to check the +5 Vdc at the RED and BRN wires; then, check the other wires. To replace DS1-DS6, rotate the metal contact to the bulb out of the way and remove the bulb from rear of board.

Table 8-6. A11 Exponent/Measurement Unit Selection

E-COUNT	S7 POSITION	IC14 (ABCD)	J2 OUTPUTS	A13 LAMP STATUS			
				MHz	kHz	Hz	RPM
8	Hz	HHHL	A = H, B = L I = L, D = H	ON	OFF	OFF	OFF
	RPM	N/A	N/A	N/A	N/A	N/A	N/A
7	Hz	LLLH	A = L, B = H I = H, D = L	ON	OFF	OFF	OFF
	RPM	Same	Same	OFF	OFF	OFF	ON
6	Hz	HLLH	A = H, B = H I = H, D = L	ON	OFF	OFF	OFF
	RPM	Same	Same	OFF	OFF	OFF	ON
5	Hz	LHLH	A = L, B = H, I = H, D = H	OFF	ON	OFF	OFF
	RPM	Same	A = L, B = H I = L, D = H	OFF	OFF	OFF	ON
4	Hz	HHLH	A = H, B = H I = H, D = H	OFF	ON	OFF	OFF
	RPM	Same	A = H, B = H, I = L, D = H	OFF	OFF	OFF	ON
3	Hz	LLHH	A = L, B = L, I = H, D = H	OFF	ON	OFF	OFF
	RPM	Same	A = L, B = L, I = L, D = H	OFF	OFF	OFF	ON
2	Hz	HLHH	A = H, B = L, I = H, D = H	OFF	OFF	ON	OFF
	RPM	Same	A = H, B = L, I = L, D = H	OFF	OFF	OFF	ON
1	Hz	LHHH	A = L, B = H, I = H, D = L	OFF	OFF	ON	OFF
	RPM	Same	Same	OFF	OFF	OFF	ON
0	Hz	HABH	A = H, B = H, I = H, D = L	OFF	OFF	ON	OFF
	RPM	Same	Same	OFF	OFF	OFF	ON



NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS:

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
IC1,2,11,13,16	1820-0054
3-9,14	1820-0116
10,17,19	1820-0094
12	1820-0176
15,21	1820-0069
18	1820-0119
20	1820-0077
22	1820-0328
23	1820-0068
Q1	1854-0071
2-5	1853-0020

REFERENCE DESIGNATIONS

NO PREFIX	A11	A13
J3	IC1-23 J1,2 Q1-5 R1-6	DS1-6
S5		

Figure 8-13. A11 Main Board Assy  
A13 Annunciator Board Assy  
(Sheet 2 of 2)

A14 OPERATION

This assembly includes a 10 MHz oscillator, 10 MHz multiplier, output one-shot multivibrator and a driver. Oscillator frequency and crystal current are adjusted by C5 and R6 respectively. The oscillator section consists of Q1, Q2 and Q3. The multiplier section consists of two tuned amplifiers whose output is shaped by Q7 and Q8. Driver Q9 provides positive pulses at pin 3. With TIME BASE switch S3 set to EXT, operating voltage for the oscillator is disconnected, and an external standard frequency (1, 2.5, 5, or 10 MHz) may be connected to the time base INPUT connector, J1, on rear panel.

A14 TROUBLESHOOTING

Measure dc voltages coming into the board (+12V at pin 14, -12V at pin 15, and +5.1V at pin 4). Make waveform measurements to determine which stage is not operating. If oscillator section is not working, try adjusting RG following adjustment procedure below. If the preceding checks fail to locate the problem, replace 10 MHz crystal (part of A15). NOTE: Whenever crystal is changed, RG and C5 must be adjusted. Be sure to use a 50:1 attenuator probe when making waveform measurements.

A14 ADJUSTMENTS

- a. L2, 3, 4, and 5 adjustment:
  1. Set TIME BASE switch to EXT
  2. Connect 1 MHz standard to time base INPUT jack on rear panel.
  3. Connect oscilloscope through 50:1 probe to pin 1. NOTE: Do not use extender board during adjustment procedure.
  4. Adjust L2, 3, 4, and 5 for maximum output (should be greater than 0.7 Vrms, 2V peak-to-peak).
- b. RG and C5 Adjustment:
  1. Set TIME BASE switch to INT.
  2. Connect an electronic counter to TIME BASE INPUT jack on rear panel.
  3. Adjust C5 for 10 MHz ( $\pm 11$  Hz). NOTE: If crystal or heater (A15 Assembly) has been changed it may be necessary to select C4 to permit oscillator tuning to 10 MHz.

4. Clip a current probe over the orange wire coming from pin 12. Connect probe through probe amplifier to oscilloscope. Set oscilloscope to .05V/cm and probe amplifier to 5 mA/cm.
5. Adjust R6 for 20 mA P-P on oscilloscope.
6. Readjust C5 for 10 MHz  $\pm 1$  count on test counter.

COUNTER SETTINGS

MODE . . . . . NORM  
MEASUREMENT TIME . . . . . .1  
TIME BASE . . . . . INT

All waveforms taken with HP 175A Oscilloscope and HP 10002A 50:1 Divider Probe. Center line of graticule is zero volts.

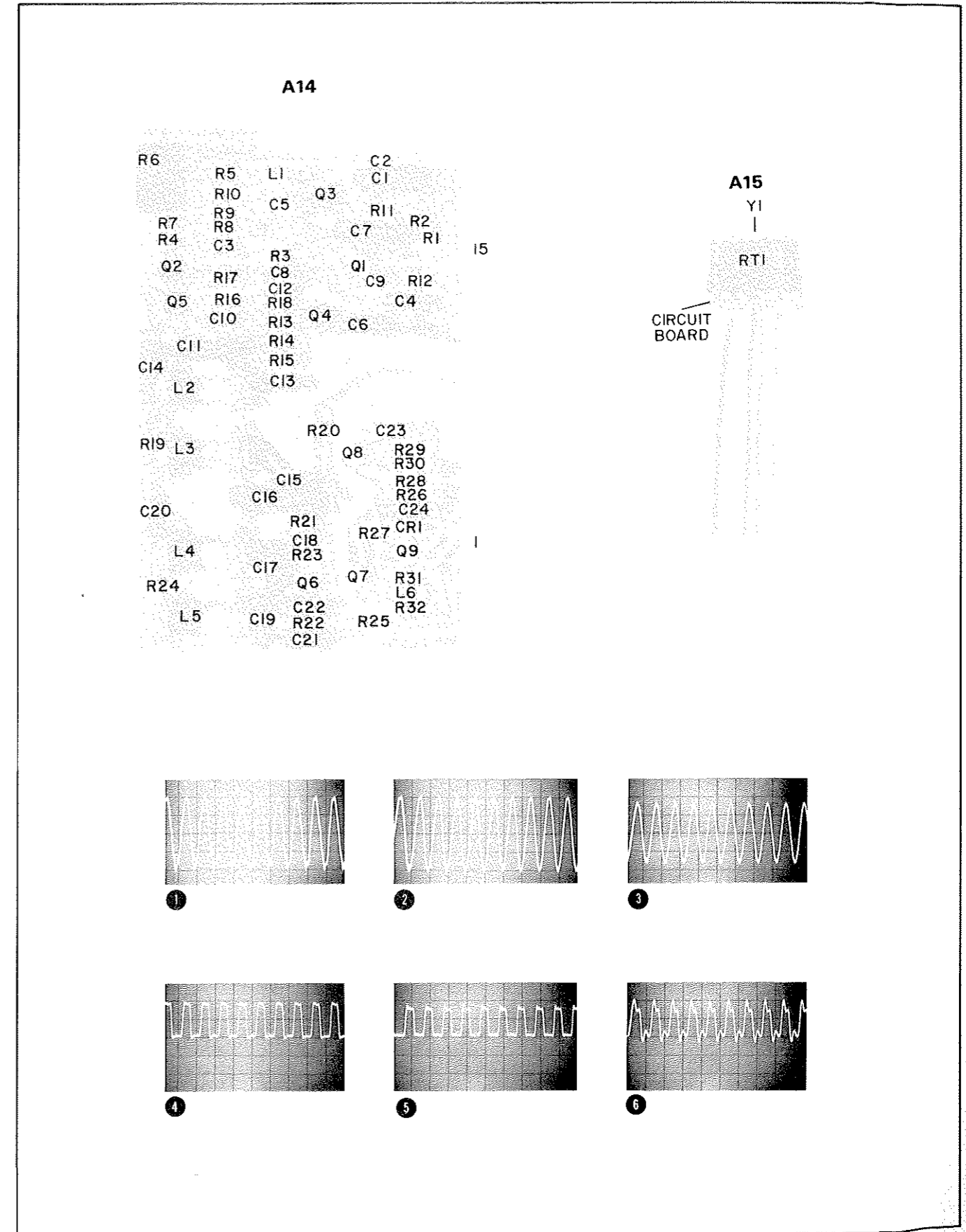
WAVEFORM NO.	Oscilloscope Settings				
	SENS V/CM	AC	DC	SLOPE + -	SWEEP /CM
1	.005	x		x	.1 $\mu$ S
2	.02	x		x	.1 $\mu$ S
3	.02		x	x	1 $\mu$ S
4	.05		x	x	.1 $\mu$ S
5	.05		x	x	.1 $\mu$ S
6	.02		x	x	.1 $\mu$ S

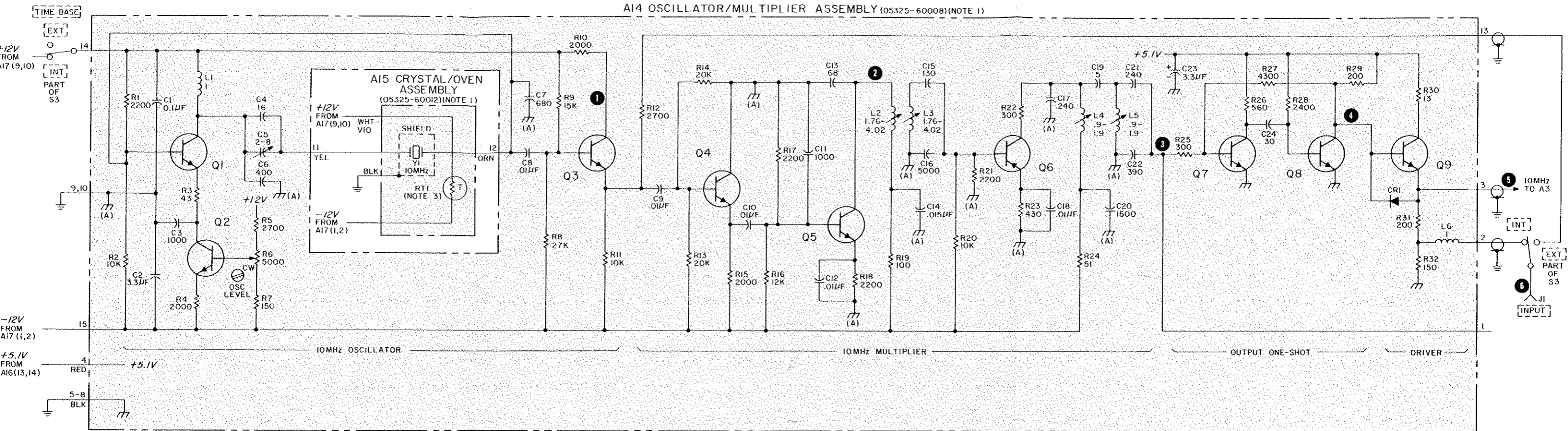
A15 OPERATION

This assembly contains the 10 MHz crystal for A14, and heater RT1 which maintains crystal temperature. The heater operates on 24 volts (+12V and -12V supplied by A17).

A15 TROUBLESHOOTING

If oscillator frequency will not stay within specified limit, it may be due to a faulty heater. Check resistance of RT1 (should be 60 to 80 ohms at room temperature). If heater check is satisfactory, replace crystal.





**NOTES**

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED:  
RESISTANCE IN OHMS;  
CAPACITANCE IN PICO FARADS;  
INDUCTANCE IN MICROHENRIES
3. RESISTANCE OF HEATER ELEMENT SHOULD BE BETWEEN 60 AND 80Ω AT ROOM TEMPERATURE WITH NO POWER APPLIED

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
CR1	1910-0022
Q1	1854-0019
2-4	1854-0071
5,6	1853-0036
7	2N3906
	1854-0005
	2N708
8,9	1854-0009
	2N709

REFERENCE DESIGNATIONS

NO PREFIX	A15	A14
J1		C1-24 CR1
S3	RT1	L1-6 Q1-9 R1-32
	Y1	

05323 D-15

Figure 8-14. A14 Oscillator/Multiplier Board Assy  
A15 Crystal/Oven 10 MHz Assy

A16 OPERATION

This circuit supplies +175V and +5.1 Vdc. The +175V supply is series regulated and operates the digital display tubes in A12. The +5.1V supply is used to supply the integrated circuits and A13 lamps. The +5.1V supply is series regulated and receives operating bias from the -12V supply on A17. Q1 is located on the rear panel of the Counter.

A16 TROUBLESHOOTING

Make voltage and resistance measurements. If trouble is encountered with the +5.1V supply, check to see that -12V bias is at pin 15.

WARNING

USE EXTREME CAUTION WHEN TROUBLESHOOTING THIS ASSEMBLY AS +175 VOLTS IS PRESENT AT MANY POINTS ON BOARD.

A17 OPERATION

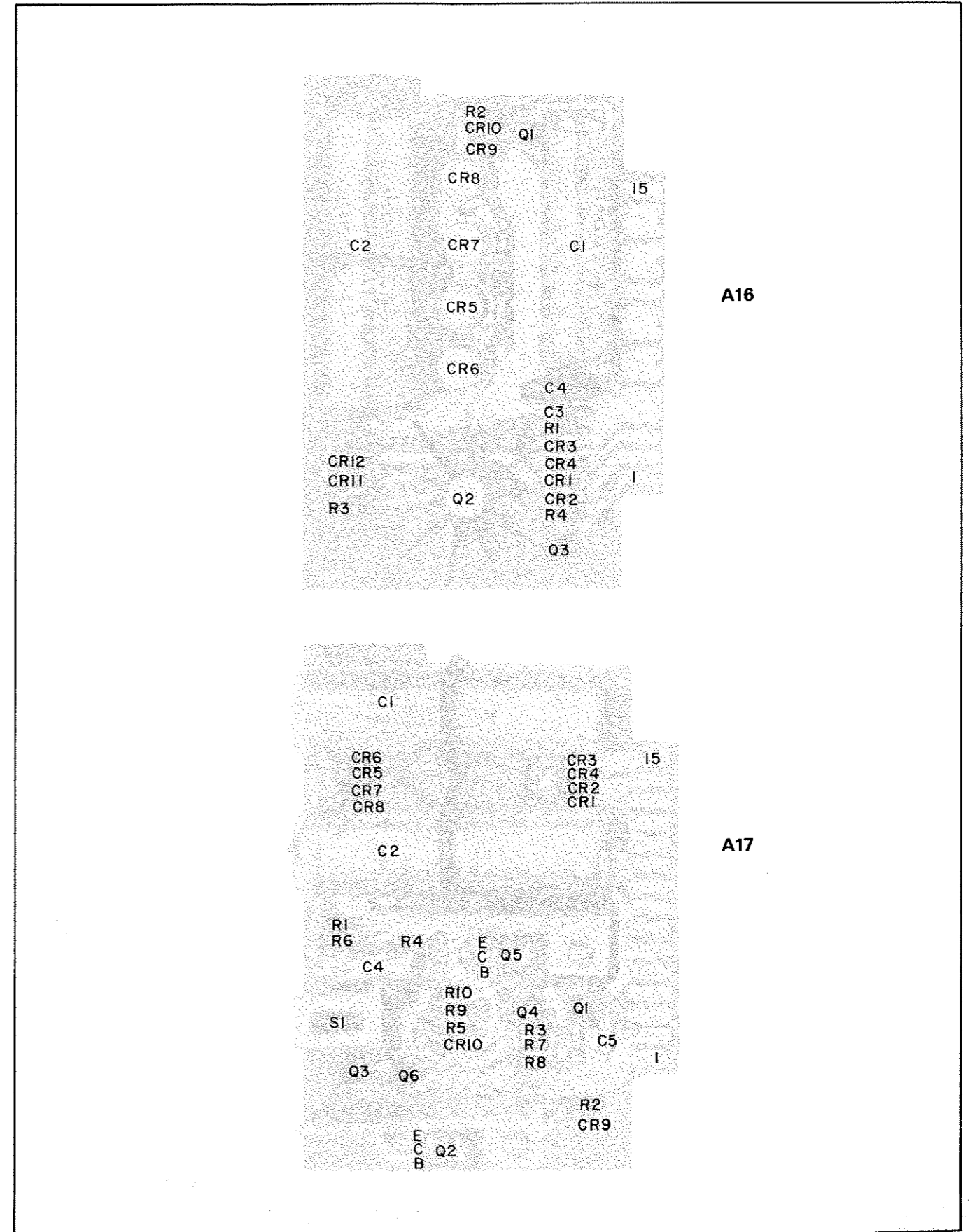
This assembly supplies +12V and -12V. The two regulator circuits depend on each other for operating bias. The -12V supply also gives bias to the +5.1V regulator on A16. If the +12V or -12V regulator is overloaded, it will turn off the other regulator. This, in turn, will shut off the regulator being overloaded. To restore power, reset switch S1 must be momentarily closed (push down), or AC line voltage interrupted.

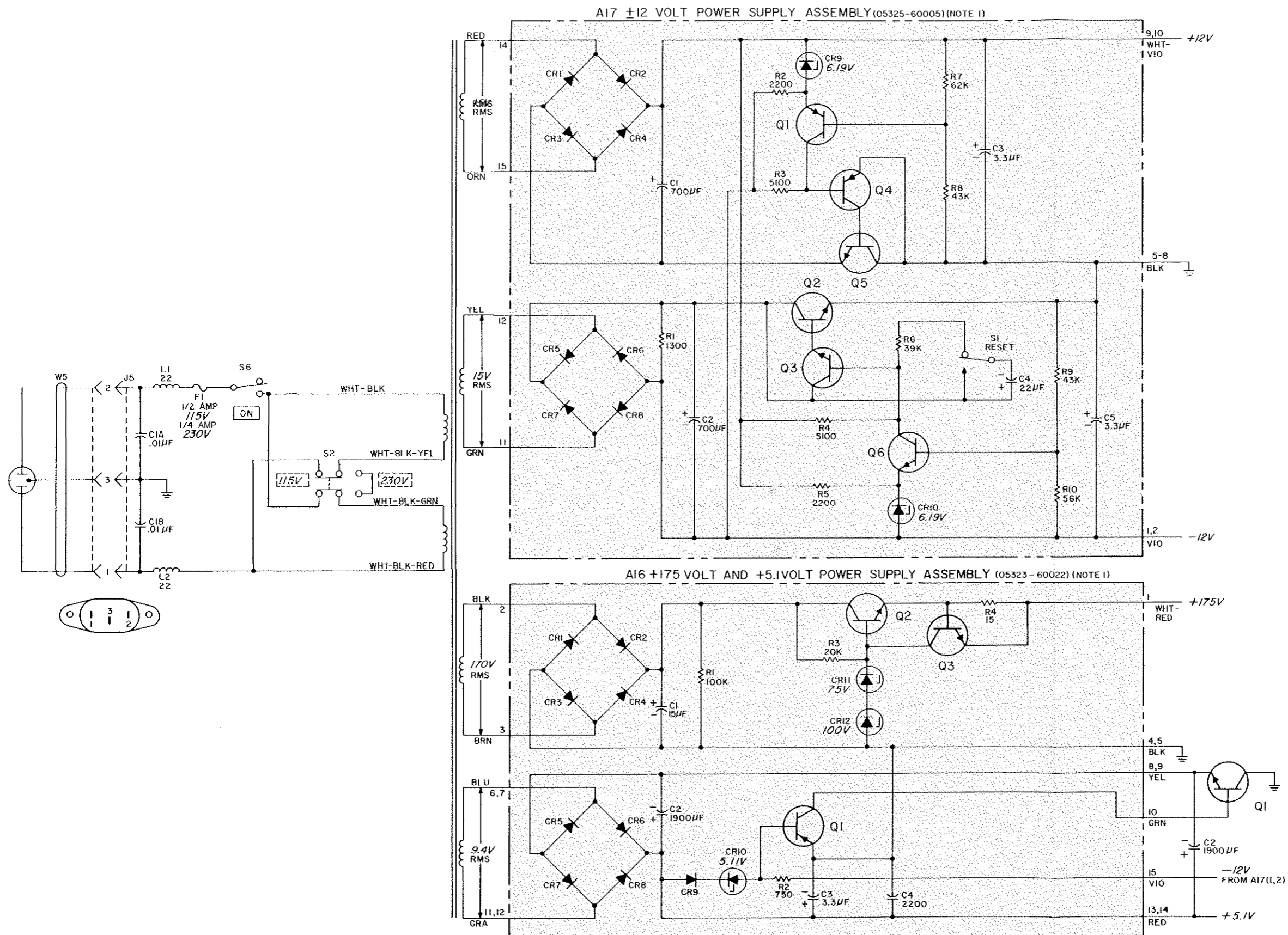
A17 TROUBLESHOOTING

If there is no output, try pushing reset switch S1 on board. If supply does not restart, alternately disconnect leads from XA17 (pins 9, 10, and 1, 2) while trying reset switch again. Make resistance measurements to check diodes and transistors.

CAUTION

Do not short metal plates protruding from board. These are heat sinks for A17Q2 and Q5 and are "Hot" to the collectors of these transistors.





NOTES

1. REFERENCE DESIGNATIONS WITHIN THIS ASSEMBLY ARE ABBREVIATED. ADD ASSEMBLY NUMBER TO ABBREVIATION FOR COMPLETE DESCRIPTION.
2. UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS, CAPACITANCE IN PICOFARADS, INDUCTANCE IN MICROHENRIES

TABLE

REFERENCE DESIGNATIONS	HP PART NUMBERS
A17	
CR1-8, 9,10	1901-0049
Q1,4	1902-3114
2,5	1853-0020
3	1854-0300
	1854-0071
A16	
CR1-4	1901-0028
5-8	1901-0200
9	1901-0040
10	1902-3094
11	1902-3429
12	1902-3394
Q1	1853-0020
2	1854-0232
3	1854-0071
NO PREFIX	
Q1	1854-0063
	2N3055

REFERENCE DESIGNATIONS

NO PREFIX	A17	A16
L1,2	CR1-10	CR1-12
S2,6	Q1-6	Q1-3
T1	R1-10	R1-4
W5		

Figure 8-15. A16 +5.1V/7-175V Power Supply



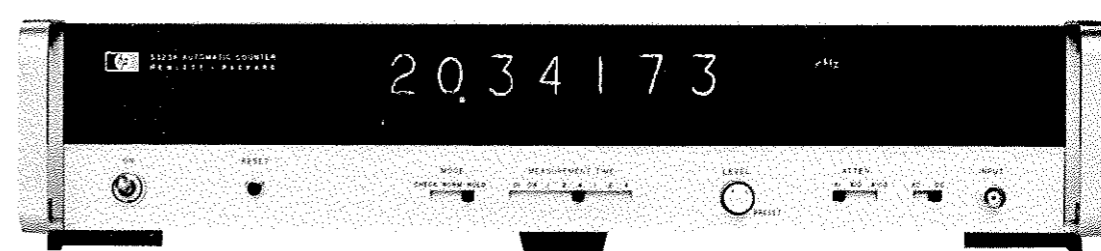


HP 5323A

AUTOMATIC COUNTER 5323A

# AUTOMATIC COUNTER 5323A

OPERATING AND SERVICE MANUAL



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